INTEGRATED CIRCUIT AND SYSTEM DESIGN FOR COGNITIVE RADIO AND ULTRA-LOW POWER APPLICATIONS

A Dissertation

by

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Submitted to the Office of Graduate and Professional Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

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December 2017

Major Subject: Electrical Engineering

ABSTRACT

The ubiquitous presence of wireless and battery-powered devices is an inseparable and invincible feature of our modern life. Meanwhile, the spectrum aggregation, and limited battery capacity of handheld devices challenge the exploding demand and growth of such radio systems. In this work, we try to present two separate solutions for each case; an ultra-wideband (UWB) receiver for Cognitive Radio (CR) applications to deal with spectrum aggregation, and an ultra-low power (ULP) receiver to enhance battery life of handheld wireless devices.

Limited linearity and LO harmonics mixing are two major issues that ultra-wideband receivers, and CR in particular, are dealing with. Direct conversion schemes, based on current-driven passive mixers, have shown to improve the linearity, but unable to resolve LO harmonic mixing problem. They are usually limited to 3^{rd}, and 5^{th} harmonics rejection or require very complex and power hungry circuitry for higher number of harmonics. This work presents a heterodyne up-down conversion scheme in 180 nm CMOS technology for CR applications (54-862 MHz band) that mitigates the harmonic mixing issue for all the harmonics, while by employing an active feedback loop, a comparable to the state-of-the art IIP_3 of better than +10 dBm is achieved. Measurements show an average NF of 7.5 dB when the active feedback loop is off (ie. in the absence of destructive interference), and 15.5 dB when the feedback loop is active and a 0 dBm interferer is applied, respectively.

Also, the second part of this work presents an ultra-low power super-regenerative receiver (SRR) suitable for OOK modulation and provides analytical insight into its design procedure. The receiver is fabricated in 40 nm CMOS technology and operates in the ISM band of 902-928 MHz. Binary search algorithm through Successive Approximation Register (SAR) architecture is being exploited to calibrate the internally generated quench

signal and the working frequency of the receiver. Employing an on-chip inductor and a single-ended to differential architecture for the input amplifier has made the receiver fully integrable, eliminating the need for external components. A power consumption of 320 μW from a 0.65 V supply results in an excellent energy efficiency of 80 pJ/b at 4 Mb/s data rate. The receiver also employs an ADC that enables soft-decisioning and a convenient sensitivity-data rate trade-off, achieving sensitivity of -86.5, and -101.5 dBm at 1000 and 31.25 kbps data rate, respectively.

DEDICATION

To my parents.

ACKNOWLEDGMENTS

Firstly, I would like to express my sincere gratitude and deep appreciation to my research advisor Professor Dr. Kamran Entesari, you have been a tremendous mentor for me. I would like to thank you for encouraging my research and for your patience and support at the times of hardship. Your advice on both research as well as on my career have been priceless. I would also like to thank my committee members, Professor Jose Silva Martinez, Professor Sunil Khatri, and professor Ben Zoghi for serving as my committee members. I also want to thank you for letting my defense be an enjoyable moment, for your insightful comments and encouragement, but also for the hard question which led me to widen my research from various perspectives, thanks to you.

I thank my fellow friends in the AMSC, in particular Masoud Moslehi Bajestan for the stimulating discussions, and for the sleepless nights we were working together before deadlines. I would also like to thank Hajir Hedayati, Ehsan Zhian Tabassy, Alireza Pourghorban Saghati, Shokoufeh Arbabi, Ali Pourghorban Saghati for all their help and all the fun we have had in the past several years.

Last but not the least, I would like to thank my family; my parents and to my brothers for supporting me spiritually throughout writing this thesis and my life in general.

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1. INTRODUCTION

In this work we try to address two of the major challenges of the modern area wireless communications; spectrum aggregation, and limited battery capacity. These two issues are inherently different, therefore we deal with each case independently in a separate chapter. This chapter however, introduces and describes these challenges in more generic terms and justifies the motivation to tackle these issues from the presented perspective. The technical introduction and pertaining literature review of the subject is presented in Chapter 2, and 3.

1.1 Dynamic Spectrum Access Network (DSAN) and Cognitive Radio (CR)

At the dawn of wireless radio communications, in early 1920s, there was no regulatory organization to standardize and manage utilization of the radio spectrum. Different users had to compete, by increasing their transmission power level, to seize their desired frequency band. Eventually this situation resulted in high interference levels, and led to the advent of independent regulatory organization, e.g. Federal Communications Commission (FCC) in 1934, to guarantee efficient and affective use of the available spectrum, fair competition opportunities, and quality of service. The idea by which these entities tried to resolve the interference issue was to allocate certain frequencies, and transmitted-power boundaries for certain applications (licensed or primary users) [1]. Ever since, various radio communication systems have developed around the idea of low-interference regulatory by means of dedicating exclusive right of use for each particular communication system, e.g. TV broadcasting, mobile, and satellite communications.

This approach has resulted in a strictly congested allocation of frequency bands, in which free and unlicensed bands have become scarce, where unlicensed (secondary) users are striving to use spectrum. Fig. 1.1 illustrates the UHF[1] band of the radio spectrum and

[1] 300 MHz to 1 GHz, as defined by IEEE.

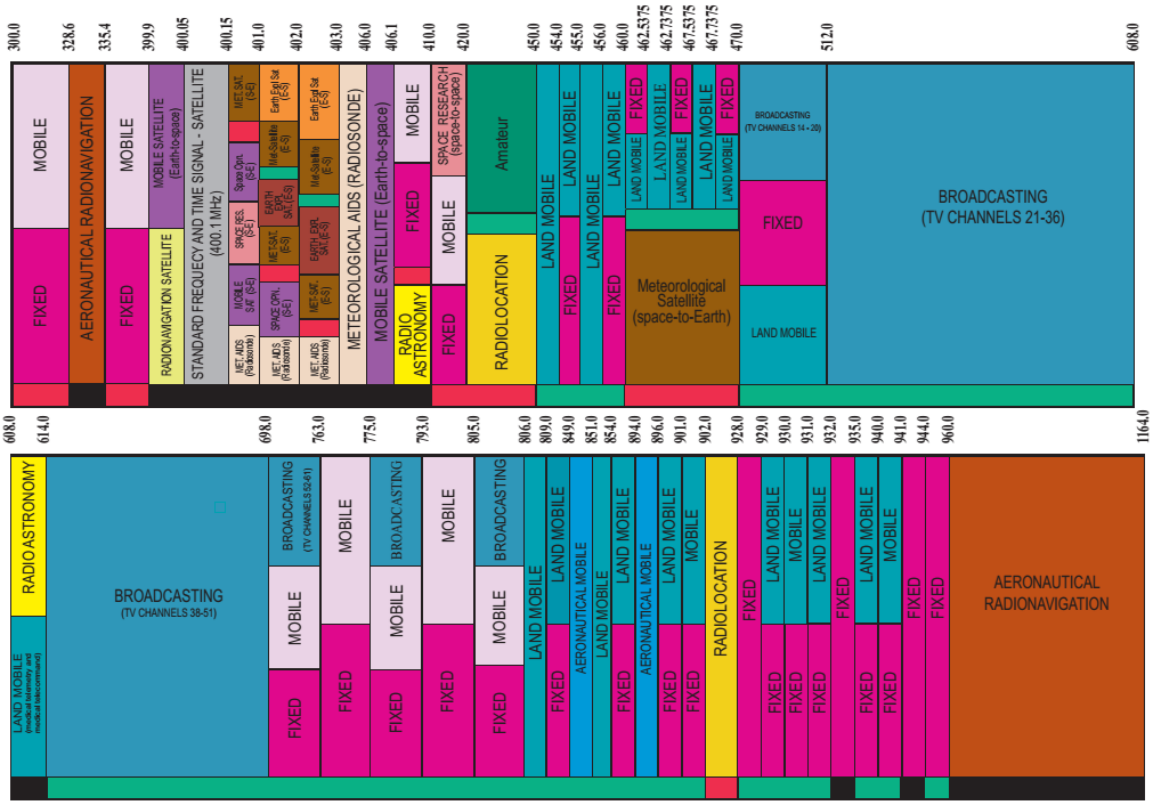


Figure 1.1: United States Frequency Allocations Chart; The Radio Spectrum (UHF band) [3].

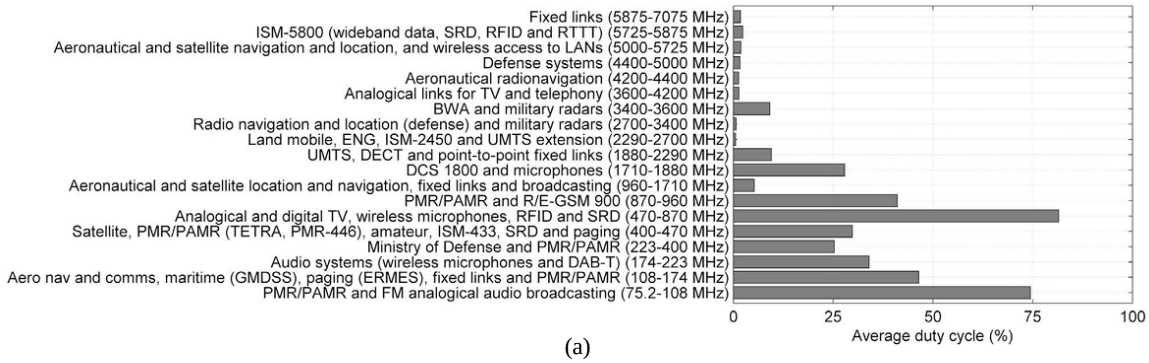
demonstrates how congested it has become [3]. The UHF band, in particular, is more appealing for long range communication systems, since the spectrum has a better propagation characteristics in this frequency range [4], and at the same time integrated systems can be implemented to set up radio communications with multi-MHz bandwidth. On the other hand, Fig. 1.1 suggests there is little to no hope for any unlicensed or secondary user to utilize this precious part of the spectrum.

In spite of mitigating interference problem, the current spectrum allocation approach is shown not to be highly inefficient when it comes to the spectrum utilization. This has resulted in significant underutilization of spectrum, while the demand for the spectrum is ever more increasing. Several new studies and surveys have shown [1,2,5–7] that although

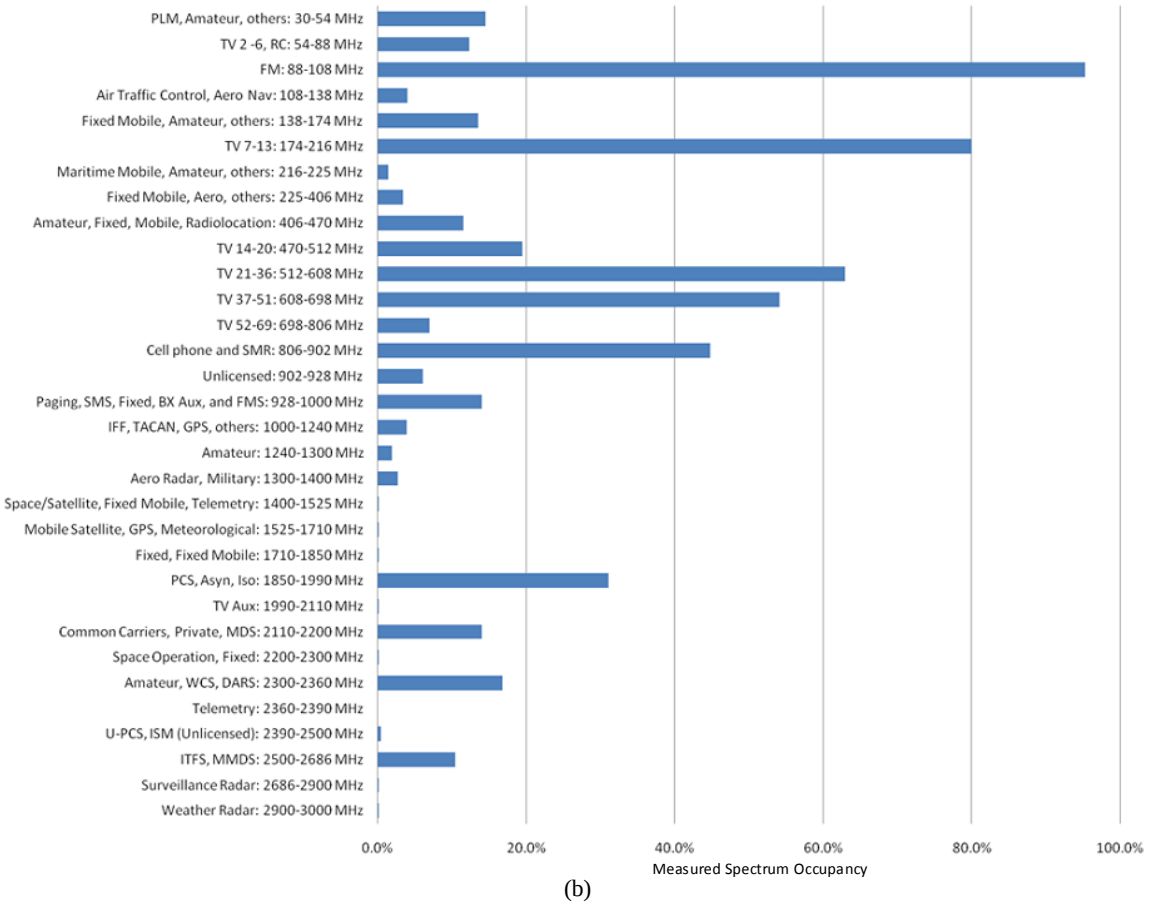
almost all RF spectrum is allocated, most of it is either unused or underutilized, emphasizing the inefficiency of the exclusive-rights spectrum-management approach. Fig. 1.2 illustrates the average occupancy of wide portion of the spectrum over a long time [1, 2]. This results would most likely differ from place to place and time to time, however, they establish the fact that the spectrum is underutilized and call for a more agile and spectrum-aware communication approach. One way to alleviate problems caused by the lack of available allocated spectrum, is to adopt so-called dynamic-spectrum-access network (DSAN). This process should be performed in a way that does not introduce disruption for the incumbent users. In these networks, an unlicensed (secondary) user is allowed to set up a communication channel, while refraining from any destructive interference with licensed (primary) users.

The notion of Cognitive Radio (CR) was originated from Joseph Mitola's work about 2000 [8]. He identified a cognitive radio as an intelligent personal data assistant (PDA), and its underlying networks, that are computationally intelligent regarding their radio resources to detect user communications needs and provide radio resources and wireless services accordingly. Although Mitola's work focused on the application layer, many research results in physical layer have been published on this area, inspired by his idea [9, 10]. CR grew interest among communication community and led to the start of the IEEE Communications Society Technical Committee on Cognitive Networks in 2005, and culminated in 2008 by the development of IEEE 802.22 standard [11]. It opened the TV broadcasting vacant channels in the VHF and UHF bands for unlicensed applications [12]. IEEE 802.22 can be perceived as an alternative technology for IEEE 802.11, providing point-to-multipoint wireless regional area networks, and by taking advantage of better propagation characteristics of VHF, and UHF band, covering an area within a radius of 10 to 30 km.

CR concept seems a promising solution to deal with the spectrum scarcity in the era



(a)



(b)

Figure 1.2: Recent surveys of the RF spectrum reveal that the vast portion of the spectrum is underutilized. Graphs are extracted from (a) [1], and (b) [2].

that demand for more radio links is exploding, however, there have remained serious challenges in the way of its implementation. CR under standard IEEE 802.22, by nature is an

ultra-wideband (UWB) receiver, suffering from all of UWB receivers design challenges, particularly out-of band interference. The fact that this standard tries to utilize the lower end of the spectrum (due to its superior propagation characteristics) exacerbates these challenges, especially by bringing in the problem of harmonics mixing, a phenomenon that is not as crucial and disruptive in other UWB systems, such as Software-Defined Radios (SDR). Chapter 2 focuses on a design solution for a receiver that can effectively deal with these issues, that suits the CR standard.

1.2 The Need for Ultra-Low Power (ULP) Systems

The advent of Internet of Things (IoT), or Internet of Everything (IoE) notion, which revolves around machine-to-machine communications, sensor network data gathering, and cloud computing, has opened a door to evermore increasing number and possibilities of wireless and battery-powered devices. It is predicted that by 2020, number of battery-powered wireless connected devices passes beyond 50 bilion[2], mainly constituted from phones, tablets, laptops, game consoles all other types of connected small devices in areas like home automation, smart energy, elderly care at home, transportation, asset tracking and many others which will be a real candidate to be IoT devices [13, 14]. Beside an exciting landscape that this new notion promises, there still remains numerous underlying challenges that need to be overcome, in order to fully utilize all its promised potentials.

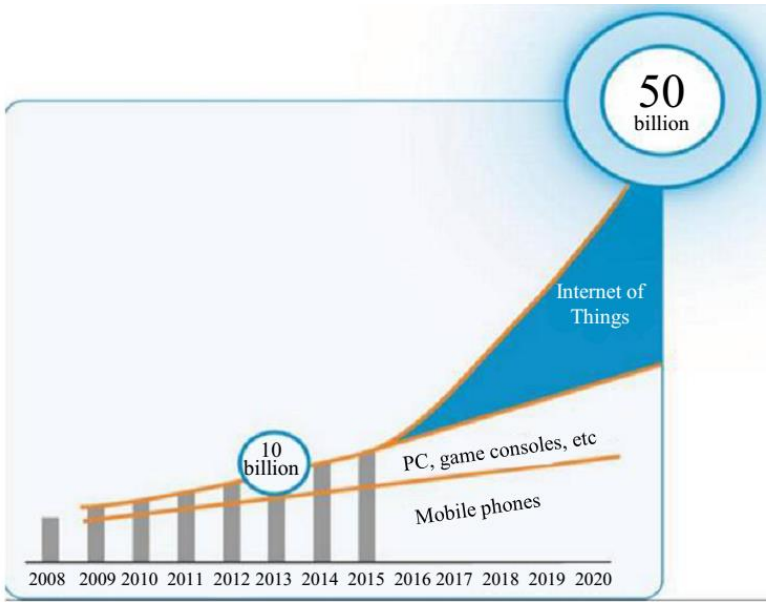
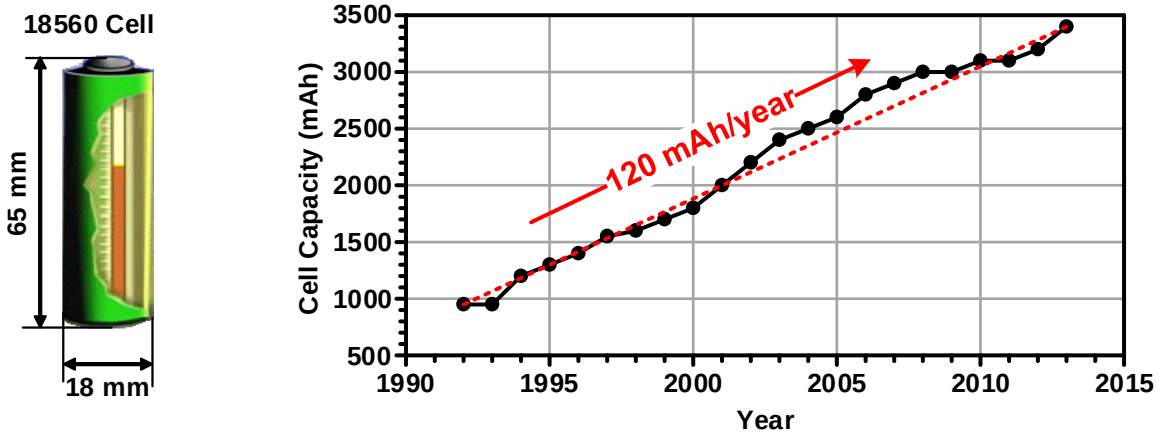


Figure 1.3: The exponential growth of mobile devices due to the advent of IoT [14].

[2]A number that was estimated to be around 10 bilion in 2013.

One major issue is the battery depletion duration of a battery-powered device. While the demand for wireless connection is increasing exponentially, the battery capacity, as shown in Fig. 1.4 has only improved linearly over the past two decades [15]. The mobile data usage in north America in 2017, is 45 times the volume of traffic in 2010 [16]. Despite the fact that the exponential growth of the accessible bandwidth has contributed to the exponential growth of mobile data consumption, it is safe to say that we have grown used to work with mobile devices more frequently. As a result, power hungry transceivers necessitate frequent charging of the mobile devices' battery.



(a) (b)

Figure 1.4: (a) 18650 Li-Ion cell, a popular battery cell for laptops and smart phones. (b) Battery cell capacity, on average, has increased by 120 mAh/year in last two decatdes [15].

In addition to the inconvenience of frequent need to charge a mobile device, there are many applications in which the mobile device is not as accessible as, for example, a smart phone. For instance, in medical implant applications in which the mobile device is implanted inside a human body, or in a wireless sensor network (WSN) where, numerous devices might have been placed in remote locations. Beside prolonging depletion of a bat-

tery, one compelling reason for an ULP transceiver is to enable employment of emerging power supply technologies, such as energy harvesting. However, the current energy harvesting methods have a limited yield in terms of output power [17]. Therefor designing ULP transceivers is essential to make the adoption of these energy harvesting techniques a reality.

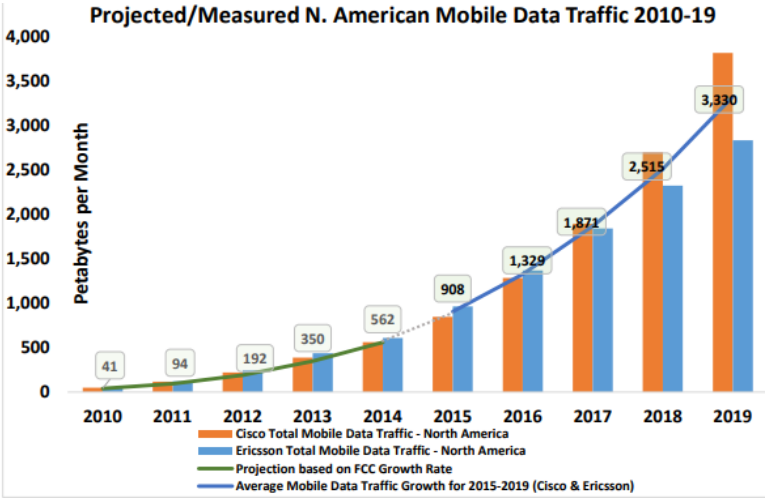


Figure 1.5: Mobile data traffic growth and projection [16].

Another potential application for ULP transceivers is wake-up radio (WUR). In order to successfully establish a communication link, the receiver end of the link should be active and listening. Since the only way to synchronize the receiver and transmitter is through the wireless link, the receiver should frequently enter an idle listening mode which waste a significant power budget of the receiver [18]. One solution that is widely being adopted to reduce this wasted idle listening power is duty cycling [19]. In this way the receiver undergoes periodic cycles of listening and turning off. Although duty cycling mitigates excessive power consumption of the idle listening mode it increases latency of the radio link and degrades its reactivity. On the other hand an ULP-WUR receiver accommodating

Table 1.1: Characteristics of various energy sources [17]

Source	Source Power	Harvested Power
Ambient Light		
Indoor	0.1 mW/cm^2	10 μW/cm^2
Outdoor	100 mW/cm^2	10 mW/cm^2
Motion/Vibration		
Human	0.5 m at 1 Hz 1 m/s^2 at 50 Hz	4 μW/cm^2
Industrial	1 m at 5 Hz 10 m/s^2 at 1 kHz	100 μW/cm^2
Thermal Energy		
Human	20 mW/cm^2	30 μW/cm^2
Industrial	100 mW/cm^2	1-10 mW/cm^2
RF		
GSM Base Station	0.3 μW/cm^2	0.1 μW/cm^2

the main transceiver can be enabled for listening continuously[3]. WUR is a narrow-band receiver, with the main goal of detecting the beacon that calls for the receiver to establish the communication link. Therefore in addition to power consumption, the other critical spec of a WUR is sensitivity, i.e. the weakest signal that a receiver is able to sense. Sensitivity of a WUR is expected to match that of the main receiver, so that employing a WUR does not limit the otherwise feasible communication range of the link.

To compare and distinguish between various ULP receivers, a widespread Figure of Merit (FoM) is being employed which takes into account a receiver's DC power consumption ($\mathrm{P_{DC}}$), sensitivity ($\mathrm{P_{Sens}}$) and Data Rate (DR) as following

$$FoM = 10\log\left(\frac{DR}{P_{DC}P_{Sens}}\right). \tag{1.1}$$

[3]Note that duty cycling is still possible, and with the expense of latency can essentially alleviate the idle listening power consumption.

In addition to power consumption and sensitivity, an ULP receiver should be low cost, and small in size in order to make WSN, or WUR a reality. Moreover, reliability, robustness, and proper performance of such receiver in presence of interferers are very important. In this work, we intend to design an ULP receiver to deliver a better or comparable to the state-of-the-art FoM, with cost, size and robustness consideration, that is a receiver with no external component or filter with precise control and calibration loops that can properly function in the presence of moderately strong interferers.

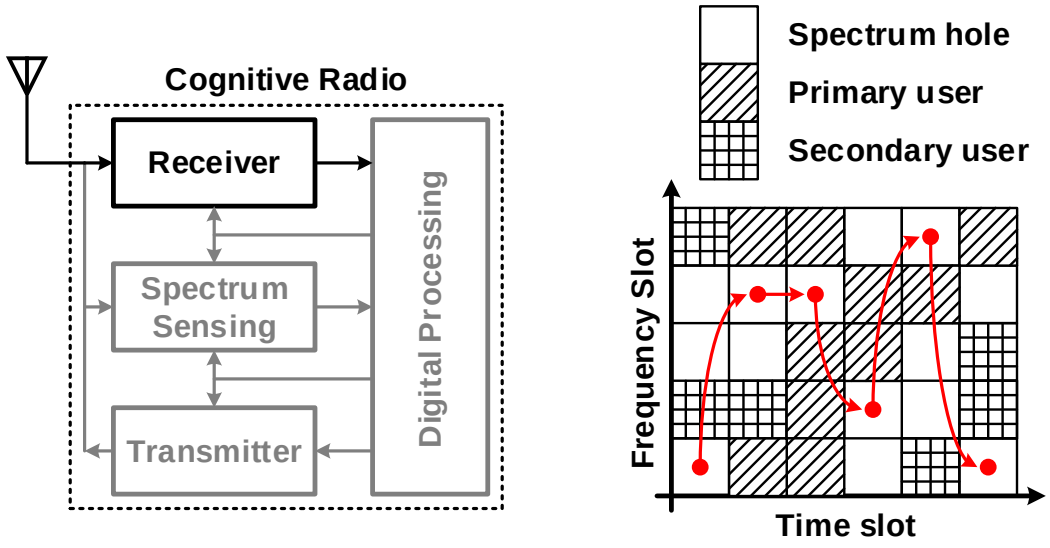
The rest of this dissertation is organized as following; Chapter 2 deals with the challenges of a CR receiver under standard IEEE 802.22, and offers a design solution, Chapter 3 describes a SR receiver as a solution to an ULP receiver need, and finally Chapter 4, concludes this work.

2. INTERFERER-TOLERANT RECEIVER FOR COGNITIVE RADIO APPLICATIONS

2.1 What is CR and What are its Challenges?

The scarcity of RF spectrum has drawn lots of attentions to new emerging frequency-agile radios, especially CR, in recent years. Although, for the most part, sub-gigahertz band is licensed for various applications, it does not mean that all the spectrum is constantly filled with radio signals [20]. The reality, in contrast, is that some licensed frequency bands in particular areas are unoccupied for most of the time, some are partially occupied and the rest are heavily used [21]. In 2008, the FCC in the United States issued a Report and Order (R&O) permitting unlicensed and cognitive use of TV white space spectrum [22]. White spaces or spectrum holes are defined as [23]: *A spectrum hole is a band of frequencies assigned to a primary user, but, at a particular time and specific geographic location, the band is not being utilized by that user.* Being a secondary user, CR should avoid interference to the incumbent broadcast services, therefore it should be comprised of a spectrum sensing module along with its radio transceiver (Fig. 2.1(a)) that incessantly monitors the spectrum, and when a primary user signal is detected, should configure the transceiver to hop to another vacant channel (ie. spectrum hole) as demonstrated conceptually in Fig. 2.1(b). In this work the focus is on presenting a solution trying to cope with the challenges that the receiver in a CR is dealing with.

The IEEE standard 802.22 is developed for the Wireless Regional Area Networks (WRAN) to operate primarily in low population density area to provide broadband data network access [12]. It regulates operation of CR in TV bands, ranging from 54 up to 862 MHz, with a communication coverage expected to reach as far as 100 km. The operat-



(a) (b)

Figure 2.1: (a) Simplified block diagram of a complete CR. (b) A CR as a secondary user should only work in a way that does not interfere with a primary user. It constantly senses the spectrum and configures the transceiver to work in the available spectrum holes.

ing frequency spans about four octaves and emanates all of the ultra-wideband receivers issues, such as Local Oscillator (LO) harmonics mixing and out-of-band interference. Harmonic mixing is due to the abrupt switching behavior of the mixers and is an inherent issue in all direct conversion receivers. For ultra-wideband receiver it can be potentially a destructive phenomenon, disrupting the desired signal with interferers that are located at or near the desired signal harmonic frequencies [24]. Linearity , and in particular Out-of-Band IIP_3 (OB-IIP_3), also plays a determining role in the sensitivity of the receiver. It has been shown that even few number of interferers along with the receiver non-linearity can produce intermodulation (IM) terms that mask, otherwise available, white spaces [25].

A receiver, in general, can be characterized based on numerous features, e.g. power consumption, area, NF, linearity, integrability, harmonic rejection, etc. Some of these features affect the cost of a receiver, e.g. area, integrability, and power consumption, and

others determine its performance, or its sensitivity in particular. It will be shown in Section 2.2, that linearity and harmonic rejection of the receiver can prove to be crucial for the particular standard IEEE 802.22, especially at the lower end of the spectrum. Therefore, in this work, the point of emphasis is to design a receiver with high linearity, while at the same time addressing the harmonic mixing problem. Recently, numerous works have tried to address these issues. Targeting Software-Defined Radio applications, they mostly have focused on the linearity and NF improvement of a receiver, since the harmonic mixing is not an important phenomenon as it is in CR[1]. Nevertheless, they have shown great improvement on the linearity of an ultra-wideband receiver [27–32]. Some has shown excellent Noise Figure (NF) [33–36], or 3^{rd} and 5^{th} harmonics rejection in addition to linearity improvement [37, 38]. However, because of employing direct conversion scheme, none of these works are suitable solutions to utilize white spaces at low frequencies, due to their susceptibility toward harmonic mixing. It is important to note that for long-range radio, VHF and UHF bands are more appealing, due to a better propagation and permeation capability [4]. Therefore for a CR receiver to operate at the lower end of its regulated band, it is crucial to overcome harmonic mixing problem.

This work, which is an extended version of [39], is based on an up-down heterodyne conversion scheme [40–42]. In this way the frequency of any potential interferer can be moved arbitrarily beyond the receiving band, and therefore all the potential interferers coinciding with the LO harmonics, are filtered out and attenuated. The main goals in this design are to mitigate the harmonic mixing problem, for all the harmonics, while maintaining a comparable to the state-of-the-art linearity and NF performance. Therefore, exploiting the fact that in a CR, the spectrum is constantly being monitored, and interferers, especially if they are strong, can be located, this work employs an active feedback loop capable of filtering out an intrusive interferer that has a destructive effect on the communi-

[1]Targeted radios in most of the SDRs start from 800 MHz [26]

cating channel. The efficacy of this filtering technique can be quantified by measuring the final interfering IM3 term and expressing it in terms of IIP_3, as will be seen in Section 2.2. While Section 2.2 discusses the generic effect of non-linearity and harmonic mixing on the sensitivity of a receiver, Section 2.3 explains how harmonic mixing problem is alleviated by means of employing heterodyne conversion scheme. Section 2.4 addresses the linearity issue and demonstrates how employing an active feedback loop can remove an intruding interferer [43–45], and discusses the NF drawback associated with employing this technique. The transistor-level design of the key building blocks, and their important features are described in section 2.5. The measurement results are presented in section 2.6, and key results are compared against the state-of-the-art in section 2.7, along with a brief discussion on benefits and shortcomings of this architecture, and finally, section 2.8 concludes this chapter.

2.2 Challenges in CR Receiver Design

As mentioned briefly in the Introduction, two major issues that make CR receiver design challenging are LO harmonic mixing and linearity of the receiver, especially out-of-band intermodulation. In this section, the mechanisms through which the sensitivity of a CR receiver can potentially be degraded by these issues are clarified, and quantified for some simple scenarios.

The standard [12] has restricted a CR user to work in the vacant digital TV channels. These channels are mainly separated into two major frequency bands; 1) VHF band ranging from 54 to 216 MHz, and, 2) UHF band ranging from 470 to 890 MHz. As can be seen from Fig. 2.2(a), the VHF band is prone to the LO harmonic mixing, and depending on the desired channel frequency, harmonics 3^{rd} to 17^{th} can still be in band[2] and therefore potentially distort the signal. Even use of harmonic rejecting (HR) architectures cannot address this issue, knowing that normally these architectures attenuate only the 3^{rd} and 5^{th} harmonics, let alone that this attenuation normally does not exceed 50 dB [30, 32, 36, 38, 46]. It is important to note that rejection of higher harmonics, although to a limited extent, is still possible with the expense of more complexity and power consumption [47, 48].

The other mechanism through which the sensitivity of a CR may degrade is spectral regrowth of interferers due to the receiver nonlinearity. Fig. 2.2(b) illustrates this phenomenon, assuming a 5^{th} order non-linear receiver. As can be seen from Fig. 2.2(b), Intermodulation terms spread around the interferers and even their higher harmonics, and can potentially coincide with the desired channel and disturb the desired signal. To calculate the destructive effect of these mechanisms on the sensitivity of a receiver, the well-known sensitivity equation needs to be revised. The sensitivity of a linear receiver ($\mathrm{P_{RX,min}}$) in an

[2]Even LO harmonics are neglected, although they may exist due to mismatch and imperfect symmetry of the LO signal [24].

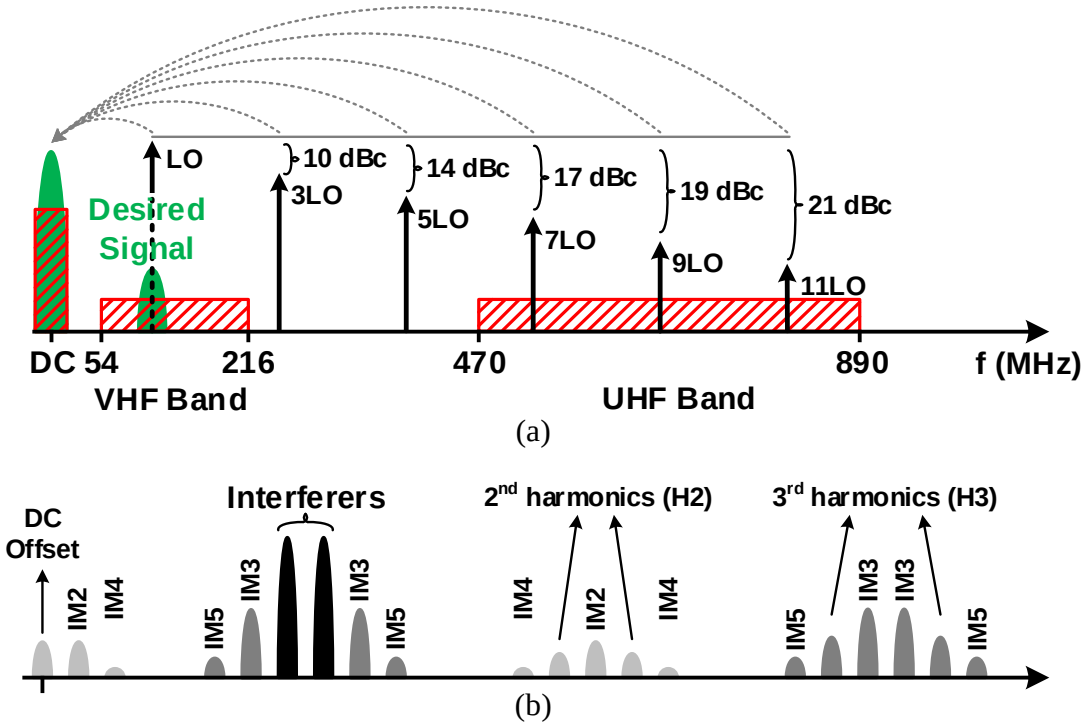


Figure 2.2: Conceptual diagram for illustrating (a) harmonic mixing, and (b) spectral regrowth due to the receiver nonlinearity.

interferer-free environment is calculated from

$$P_{RX,\min} = -174 + 10log\,(B) + SNR_{RX,\min} + NF_{RX} \tag{2.1}$$

where $\mathrm{NF_{RX}}$ is the receiver small signal NF, B is the desired signal bandwidth, and $\mathrm{SNR_{RX,min}}$ is the minimum acceptable SNR at the receiver output. According to the standard, the receiver is required to achieve a BER of better than 2×10^{-4}. Given the bandwidth of 6 MHz, for the case of QPSK modulation (rate : $\frac{1}{2}$)[3], a suggested NF of 6 dB, and 3.2 dB different margins[4], the sensitivity of the receiver, $\mathrm{P_{RX,min}}$, becomes -92.3 dBm. The

[3]According to the standard, $\mathrm{SNR_{RX,min}}$, is 4.3 and 8.1 for the case of QPSK modulation (rate: $\frac{1}{2}$), in AWGN and multipath channel, respectively. Here, the lower SNR is assumed.

[4]1.1 dB for QPSK decoder implementation, 2.1 dB accounting for the coupling loss, pre-amplification filter loss.

standard allows 1 dB of sensitivity degradation due to the presence of interferers, meaning that the non-linear sensitivity of the receiver ($\mathrm{P'_{RX,min}}$) which can be related to the linear one as in

$$P'_{RX,\min} = P_{RX,\min} + \sum (P_{IM_X,in} + P_{HM_n,in})\ (mW) \tag{2.2}$$

becomes -91.3 dBm, where $\mathrm{P_{IM_X}}$, and $\mathrm{P_{HM_n}}$ are the input-referred power of interfering $\mathrm{X^{th}}$ intermodulation and $\mathrm{n^{th}}$ harmonic mixed terms, respectively. Since the standard has put only 1 dB room for the effects of environmental interference, therefore

$$P'_{RX,\min} = P_{RX,\min} + 1 \qquad (dBm) \tag{2.3a}$$

$$P'_{RX,\min} \approx 1.25 \times P_{RX,\min} \qquad (mW) \tag{2.3b}$$

$$\sum (P_{IM_X,in} + P_{HM_n,in}) \leq \frac{P_{RX,\min}}{4} \qquad (mW). \tag{2.3c}$$

If the aggregated power of the two terms on the left side of (2.3c) exceeds the inequality, the ultimate sensitivity of the receiver ($\mathrm{P'_{RX,min}}$) starts to drop, and for stronger interferers (i.e. $\mathrm{P_{IM_X,in} + P_{HM_n,in}} \gg \frac{\mathrm{P_{RX,min}}}{4}$), it would be nonlinearity and harmonic mixing, rather than NF, limiting the receiver's overall sensitivity.

Quantifying the effect of harmonic mixing is simple; Based on the LO harmonic that might coincide with an interferer, the maximum tolerable power of that interferer can be calculated from (2.3c). For example, for receivers without HR architecture (10 dB attenuation for the 3^{rd} harmonic), and with HR architecture (assuming 45.4 dB rejection of the 3rd harmonic), $\mathrm{P'_{RX,min}}$ can be maintained in the presence of interferers up to -88.3 and -52.9 dBm, respectively. Table 2.1 demonstrates the limiting effect of harmonic mixing on the maximum tolerable interferer, up to the 9^{th} harmonic for a simple and a HR with 3^{rd} and 5^{th} harmonics cancellation[5] direct-conversion receivers, respectively.

[5]The attenuation for HR architecture is based on averaging the reported numbers in [30, 32, 36, 38, 46].

Table 2.1: Tolerable interferer level due to harmonic mixing

Harmonic No.	3^{rd}		5^{th}		7^{th}	9^{th}
HR Architecture	$\times$	$\surd$	$\times$	$\surd$	$\times$	$\times$
Attenuation (dB)	10	45.4	14	52.4	17	19
Tolerable interferer (dBm)	-88.3	-52.9	-84.3	-45.9	-81.3	-79.3

Note that for calculating tolerable interferer power in Table 2.1, the effect of IM terms are neglected and only one coinciding interferer is considered, therefore (2.3c) is simplified to $\mathrm{P_{HM_n,in}} \leq \frac{\mathrm{P_{RX,min}}}{4}$. Reader can conceive various other cases (however less probable) that multiple interferers coincide with the LO harmonics, therefore their power should be added and the tolerable interferer power becomes even smaller.

Fig. 2.2(b) shows the spectral regrowth of two interferers passing through a non-linear system of order 5, up to the 3rd harmonic frequency. To find out the non-linear sensitivity of the receiver using (2.2), the power of these IM terms should be normalized to the linear gain of the receiver, or in other word, the input-referred power of IM terms ($\mathrm{P_{IMX,in}}$, and, $\mathrm{P_{HX,in}}$) should be considered. As such, the input-referred power of the second and third IM terms will be:

$$P_{IM2,in} = 2P_I - IIP_2 \qquad (dBm) \tag{2.4a}$$

$$P_{IM3,in} = 3P_I - 2IIP_3 \qquad (dBm). \tag{2.4b}$$

By applying (2.4) into (2.3c), and neglecting the HM terms, the required linearity specs can be expressed in terms of $\mathrm{IIP_X}$, as a measure of linearity, and the interferer power $\mathrm{P_I}$

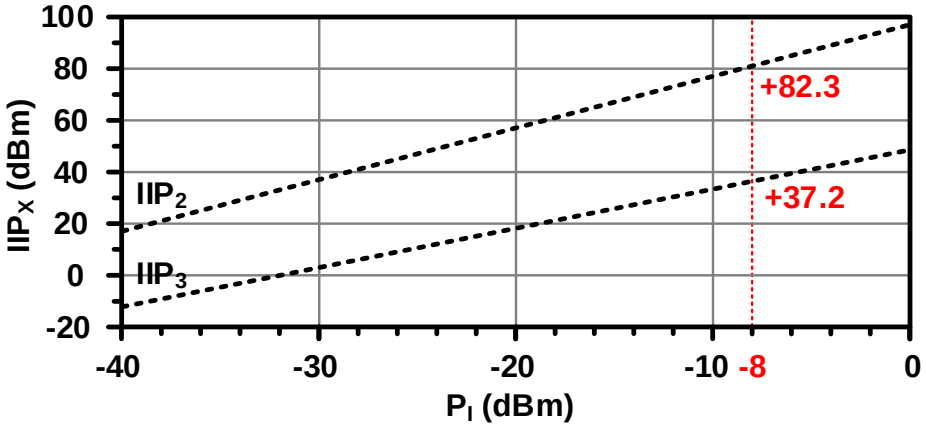


Figure 2.3: Require linearity specs ($\mathrm{IIP_X}$) Vs. interferer power ($\mathrm{P_I}$) for maintaining the linear sensitivity of the receiver ($\mathrm{P_{RX,min}} = -91.3$ dBm).

as following:

$$IIP_2 \geq 2P_I + 98.3 \qquad (dBm) \tag{2.5a}$$

$$IIP_3 \geq \frac{3}{2}P_I + 49.15 \qquad (dBm). \tag{2.5b}$$

Fig. 2.3 depicts required $\mathrm{IIP_X}$ to maintain the sensitivity required by standard (i.e. $\mathrm{P'_{RX,min}}$), versus the interferer power. It is clear that the linearity specs are stringent. For instance, to tolerate two interferers with $\mathrm{P_I} = -20$ dBm, a receiver should have $\mathrm{IIP_2}$ and $\mathrm{IIP_3}$ of better than +58.3 and +19.15 dBm, respectively. The linearity requirements are even harder to achieve for stronger interferers, considering that interferers up to -8 dBm are considered to be dealt with in this standard.

There are two important observations from the above discussion; firstly, knowing the level and location of the interferers, the linearity requirements of a receiver can be found to maintain a certain sensitivity level. Although, the standard has not described any well-defined scenario for potential interferers, which can result in significantly different receiver linearity spec, it is possible to predict the sensitivity of a receiver in different scenarios,

depending on the linearity, structure of the receiver (being susceptible to harmonic mixing or not), and the interferers strength and position in the spectrum. Secondly, although NF, linearity, and harmonic rejection, directly impact the sensitivity of a receiver, the latter two make the sensitivity unpredictable and interferer-dependent. For example, 3 dB higher NF, results in 3 dB worse sensitivity, on the other hand, sensitivity of a receiver prone to harmonic mixing degrades substantially, if there is an destructive interference.

2.3 Heterodyne-Conversion

Direct conversion schemes for ultra-wideband receivers are strongly prone to harmonic mixing problem, specially when the working band starts from very low frequencies, such as in CR standard. Unfortunately, HR architecture has a marginal effect on this problem, as discussed in the previous section. Consider the receiver in [36] (in which the frequency range spans from 80 MHz, up to 2.7 GHz) and a desired channel that is located in the VHF band. It is very likely that one of the LO harmonics[6] coincides with an interferer and distorts the signal. The solution is either to push the lower boundary of the receiver to higher frequency and spare these frequencies or to change the conversion scheme. The former solution is not appealing for this particular CR standard as the lower frequencies result in far less propagation attenuation as the communication is intended to cover as far as 100 km.

To make use of the these low frequencies, a heterodyne conversion is chosen in this design. Fig. 2.4(a) shows the simplified heterodyne system and Fig. 2.4(b) demonstrates the frequency planning in this scheme. At the first step, the desired signal is up-converted to the fixed frequency of 1 GHz. This conversion needs an LO signal capable of tuning from 1.05 to 1.85 GHz, and the potential images (IM) in this conversion, therefore lay from 2.05 to 2.85 GHz, which is outside the receiving band, and receives an attenuation of

$$Att_{IM}\left(f_I\right) = Att_{IF} + \Delta G_{LNA}\left(f_I\right) \qquad (dB) \tag{2.6}$$

where $\mathrm{Att_{IF}}$, and $\Delta \mathrm{G_{LNA}(f_I)} = \mathrm{G_{LNA}} - \mathrm{G_{LNA}(f_I)}$ are the attenuation introduced by the input filter in Fig. 2.4(a), and the LNA gain drop at $\mathrm{f_I}$, respectively. The potential LO harmonic mixing interferers at the first stage of the frequency conversion ($\mathrm{HM_{n,1}}$), will also be located outside the receiving band, ranging from 2.15 to 4.45 GHz, and 4.75 to 8.25

[6] For the worst case scenario of $\mathrm{f_s} = 80$ MHz up to the 33^{rd} LO harmonic falls in band.

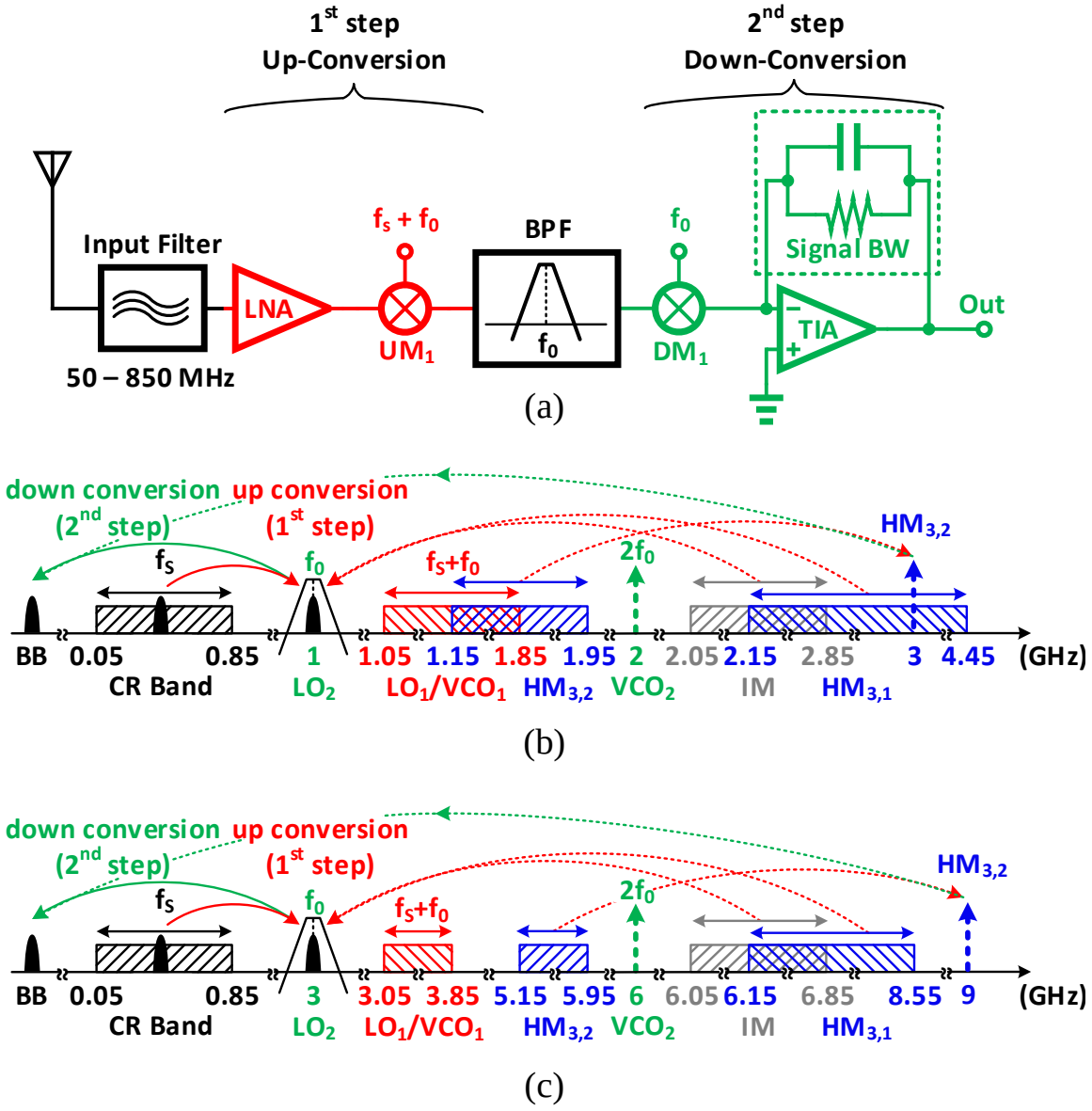


Figure 2.4: (a) Simplified structure of the heterodyne receiver. (b) Frequency planning of the heterodyne receiver, showing its immunity to LO harmonics and image mixing problems. Note that the figure is color coded, and the range of various signals are shown with different colors. (c) By increasing f_0 from 1 to 3 GHz, the potential signals that can mix with LO harmonics and distort the desired signal and the image frequency are pushed further away from the receiving band and become more attenuated. This also increases the distance between different VCOs frequencies and mitigates LO pulling issue as well.

GHz for the 3^{rd}, and 5^{th} harmonics, respectively. For instance, for the worst case scenario, that is $\mathrm{f_s} = 50\ \mathrm{MHz}$, 3^{rd} harmonic will be located at 3.15 GHz and its corresponding potential interferer at 2.15 GHz. The total attenuation that a potential interferer coinciding with the $\mathrm{n^{th}}$ LO harmonic experiences can be calculated from the following:

$$Att_{HM_{1,n}}(f_I) = Att_{IF} + 20\log(n) + \Delta G_{LNA}(f_I)\,(dB) \tag{2.7}$$

At the second step, using a constant LO frequency of 1 GHz, the desired signal is down-converted to the baseband. Note that there is no image in the second step, since it is a direct-conversion, and the harmonics, in this step ($\mathrm{HM_{n,2}}$), are located at the fixed frequencies of 3, 5, 7, ... GHz. The original frequency of the potential interferers in the second stage of frequency conversion (i.e. the frequency at the antenna) ranges from 1.15 to 1.95 and 3.15 to 3.95 GHz, for the 3^{rd}, and 5^{th} harmonics, respectively. Although closer to the receiving band, these bands experience the attenuation resulted from the BPF of Fig. 2.4(a), tuned at 1 GHz. The total attenuation for the potential interferers at this stage can therefore be calculated with the same token as:

$$Att_{HM_{2,n}}(f_I) = Att_{HM_{1,n}}(f_I) + Att_{BPF,n} \quad (dB) \tag{2.8}$$

where $\mathrm{Att_{BPF,n}}$ is the attenuation introduced by the BPF for the $\mathrm{n^{th}}$ harmonic and can be estimated from

$$Att_{BPF,n} \approx 20\log(nQ) \qquad (dB) \tag{2.9}$$

for a passive RLC network with quality factor Q $\gg$1.

The input filter can introduce as much as 40 to 50 dB attenuation for an interferer that is well beyond its pass-band [49], and the attenuation introduced by the BPF for the 3^{rd}, and 5^{th} harmonics, is around 30 and 34 dB, respectively, assuming $\mathrm{Q} \approx 10$. The 3^{rd} LO har-

monic is at least 10 dB weaker than the fundamental tone, and the LNA gain drops rapidly at high frequencies due to two main reasons; first, due to the limited bandwidth of the LNA, and second, due to input mismatch loss. At frequencies well beyond the receiving band the input impedance of the LNA, due to parasitics, goes toward short, which introduces an additional level of attenuation to the out-of-receiving-band interferers[7]. Having all that said, it can be inferred that all of the LO harmonics mixed signals can potentially be attenuated at least by 70 dB.

It is worth noting that, although the fixed LO frequency f_0 appears to be at 1 GHz, the oscillator generating it, is running at twice the frequency, since the down-conversion mixer (in contrast with the up-conversion mixer) requires 25% duty cycle clocks, and a conventional way to generate them is using a 2 GHz clock. A 2 GHz clock still might seem fairly close to the boundaries of the first step LO frequency, and therefore arises the problem of LO pulling. However, note that f_0 is a design parameter and can be arbitrarily selected. For instance, if f_0 = 3 GHz, not only the VCOs are working at a safe distance, but also the potential harmonics and images are pushed further beyond the reception band and become more attenuated as illustrated in Fig. 2.4(c). In this way the attenuation that image or harmonic mixing signals experience can be increased significantly, with a price of slightly more power consumption, since at higher frequencies the LO buffers dissipate more.

It is also worth mentioning that the two major drawbacks of employing a heterodyne scheme are having slightly higher power consumption and occupying larger area, since it requires two independent LO signals and therefore two separate VCOs. However on the other hand it enables an ultra-wideband receiver to cope with harmonic mixing issue very effectively and without complexity, as discussed in this section.

[7]In real scenarios at these frequencies the antenna pattern also gets distorted, dropping the antenna gain, however it is hard to model and is subject to variation by changing the antenna.

2.4 Active Feedback

2.4.1 Interferer Rejection

Although heterodyne conversion can alleviate the LO harmonics mixing problem, it exacerbates the nonlinearity of the receiver by adding one more stage into the receiving chain. As seen in Fig. 2.5(a), the gain of the LNA degrades the linearity of the heterodyne conversion section by amplifying the interferes, despite introducing its own non-linearity to the system. Therefore the higher boundary of the total receiver chain $\mathrm{IIP_3}$ can be found from

$$IIP_{3,tot} \leq \min\left(IIP_{3,LNA}\ ,\ IIP_{3,HC} - G_{LNA}\right) \tag{2.10}$$

where $\mathrm{IIP_{3,HC}}$, and $\mathrm{IIP_{3,LNA}}$ are the heterodyne conversion block and LNA $\mathrm{IIP_3}$, and $\mathrm{G_{LNA}}$ is the LNA gain in dB.

An approach similar to [50] has been taken to maximize the linearity of frequency conversion block, and will be discussed in details in Section 2.5. To reject or in other words filter out the interferers, the LNA is embedded inside an active feedback loop, similar to [44]. Active feedback has shown [43, 45] to have significant impact on enhancing the interference resilience of a receiver, especially for strong interferers. Fig. 2.5(b) depicts an amplifier placed in an active feedback loop. The fundamental concept behind this configuration is simple; assume an interferer is located at $\mathrm{f_{I1}}$, the active feedback path down-converts the interferer using $\mathrm{DM_2}$ and filters out every other signals through LPF. The interferer then is up-converted to its original frequency by means of $\mathrm{UM_2}$ and applied to the negative input port of the LNA, appearing as a common-mode signal. Finally, the interferer is attenuated by common-mode rejection of the differential LNA. The active feedback path actually emulates a tunable active bandpass filter (BPF), while providing a large quality factor. For instance, the equivalent BPF, shows a quality factor of around 450 when $\mathrm{f_{I1}}$= 450 MHz, and $\mathrm{f_c}$= 500 kHz.

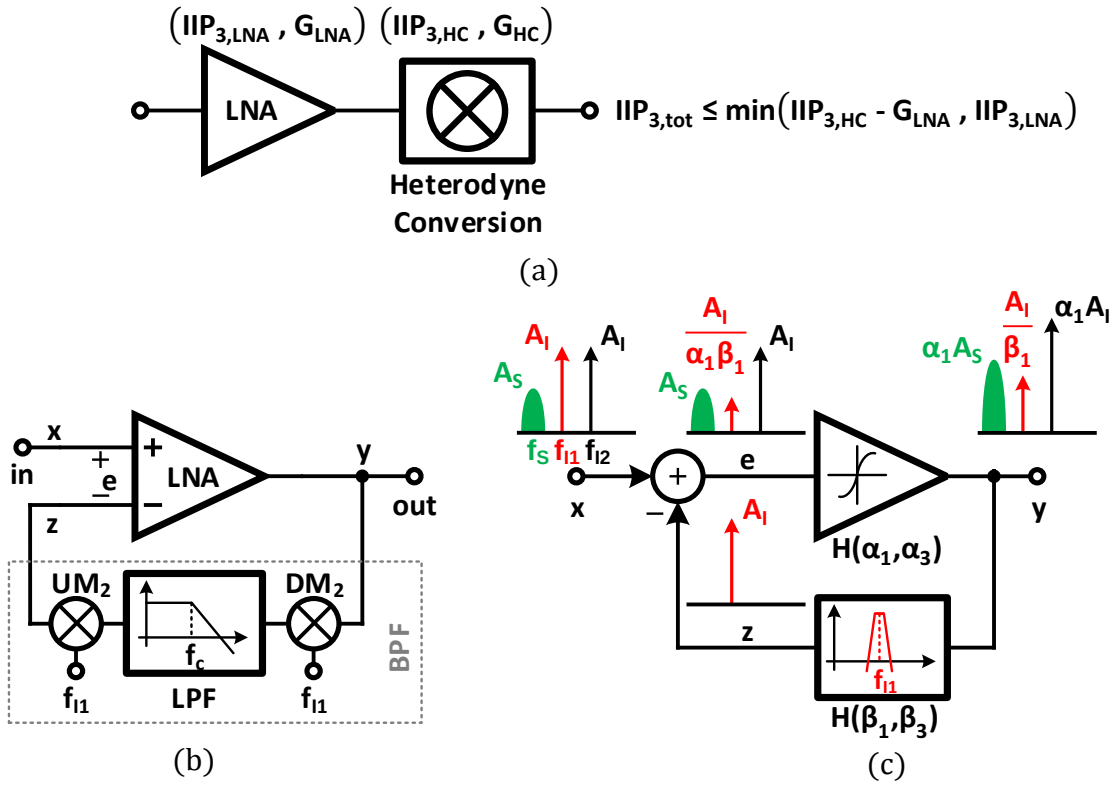


Figure 2.5: (a) Effect of cascading LNA and Heterodyne-Conversion block on the linearity of the receiver. (b) A conceptual structure of an LNA within an active feedback loop. (c) block diagram representation of the active feedback system shown in (b) illustrating different signals levels at different nodes.

Fig. 2.5(c) depicts different signals at each node while the active feedback loop is working. Appendix A deals with the more rigorous modeling of such a system, but for now, we assume that the loop can attenuate one of the interferers as much as its linear loop gain, i.e. $\alpha_1\beta_1$[8]. Since the interferer has become attenuated in this fashion, it will produce smaller IM3 term at the output, and consequently a smaller input referred IM3 term at the input. Recalling (2.2), this can be inferred that employing the active loop enhances the interference tolerance of the receiver. Although the active feedback is not a generic

[8]Note that the amplitude of the interferer would be $\alpha_1 A_I$ if the loop is inactive, and reduces to $\frac{A_I}{\beta_1}$ when the loop is activated.

linearity improvement technique, the benefit of employing it can be described in terms of $\mathrm{IIP_3}$ enhancement:

$$IIP_{3,tot,AF} = IIP_{3,tot} + T \qquad (dB) \tag{2.11}$$

where $\mathrm{IIP_{3,tot,AF}}$, and $\mathrm{IIP_{3,tot}}$ are the $\mathrm{IIP_3}$ of the receiver when the active feedback is on and off, and T is loop gain.

2.4.2 NF Penalty

Employing the active feedback loop comes with the price of worse NF. Considering Fig. 2.6, the source of this NF degradation can be understood; in a conventional receiver, various blocks are cascaded, therefore the output noise of each block is divided by its gain to be referred to the output of the preceding stage and ultimately to the source, however in this case the output noise of the up-converting mixer $\mathrm{UM_2}$ is directly applied to the input of the LNA. The NF of the whole receiver (including the active feedback loop) can be calculated as

$$NF_{tot} = NF_{LNA} + \frac{NF_{HC}}{{G_{LNA}}^2} + \frac{1}{2}\frac{\overline{V^2_{n,out,UM_2}}}{4KTR_S} \tag{2.12}$$

where, $\mathrm{NF_{HC}}$ is the NF of the heterodyne conversion block, and $\overline{\mathrm{V^2_{n,out,UM_2}}}$ is the total noise power at the output of $\mathrm{UM_2}$. Note that $\overline{\mathrm{V^2_{n,out,UM_2}}}$ should be measured at the desired signal frequency which is far enough from the LO frequency of $\mathrm{UM_2}$ (i.e. $\mathrm{f_{I1}}$) where the up-converted flicker noise of $\mathrm{UM_2}$ has rolled off. Also, note that the LPF in the feedback path attenuates the incoming noise at the desired signal frequency (along with the signal itself). However the total noise power at the output of $\mathrm{UM_2}$ is still significant. Fig. 2.7 depicts the simulated spectral noise power at the output of $\mathrm{UM_2}$, while the preceding stages in the feedback path are also considered. The LO frequency of $\mathrm{UM_2}$ (i.e. $\mathrm{f_{I1}}$, the interferer frequency) is set at 100 MHz. The flicker noise also appears at the LO harmonics but with much narrower bandwidth. For example the flicker noise contribution exceeds the

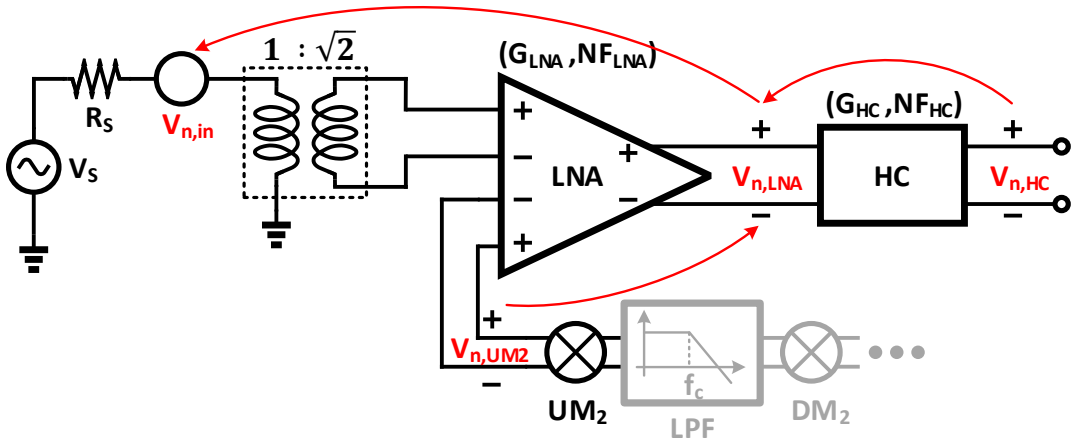


Figure 2.6: Simple model illustrating different noise sources in the receiver.

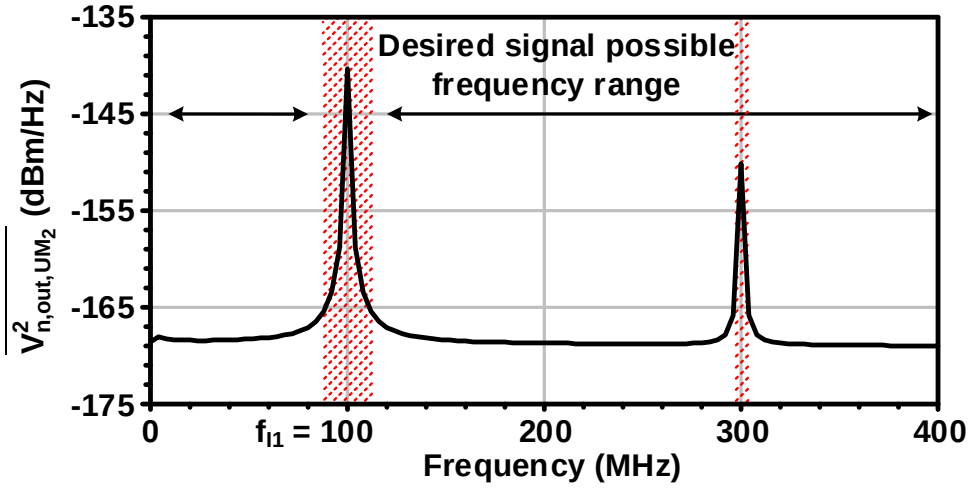


Figure 2.7: Simulated output noise power of UM2. The dashed area indicates regions that flicker noise dominates.

noise floor at the first, third, and fifth harmonics of the LO for around 26, 9, and 8 MHz, respectively.

Considering (2.12), there is a factor of $\frac{1}{2}$ beside $\overline{\mathrm{V}^2_{\mathrm{n,out,UM_2}}}$ attenuating it while referring to the input that can be understood from Fig. 2.6. Due to the differential power splitter, gain of the LNA, seen from the input source $\mathrm{V_S}$ to its output is 3 dB higher than the gain of seen from the differential output of $\mathrm{UM_2}$.

2.5 Transistor-Level Design

Fig. 2.8 illustrates the complete block diagram of the interferer-tolerant receiver, shown in single-ended fashion for simplicity. The active feedback path, In order to work properly and be stable, needs to be a quadrature path. Utilizing the spectrum sensing capability of a CR which is an inseparable part of the radio, the active loop is always set to work at the interferer frequency (i.e. f_{I1}). In case there is no destructive interferer in the spectrum, the loop can be turned off, improving NF and reducing power consumption of the receiver. The receiver requires three VCOs to provide LO signals for the mixers in the 1) active loop (DM_2, and UM_2), 2) up-conversion part (UM_1), and 3) down-conversion part (DM_1) of the heterodyne conversion block. The VCOs providing LO signals for the loop and down-conversion part of the heterodyne-conversion block are working at twice the required frequency, so that quadrature LO or 25% duty cycle clocks can be generated.

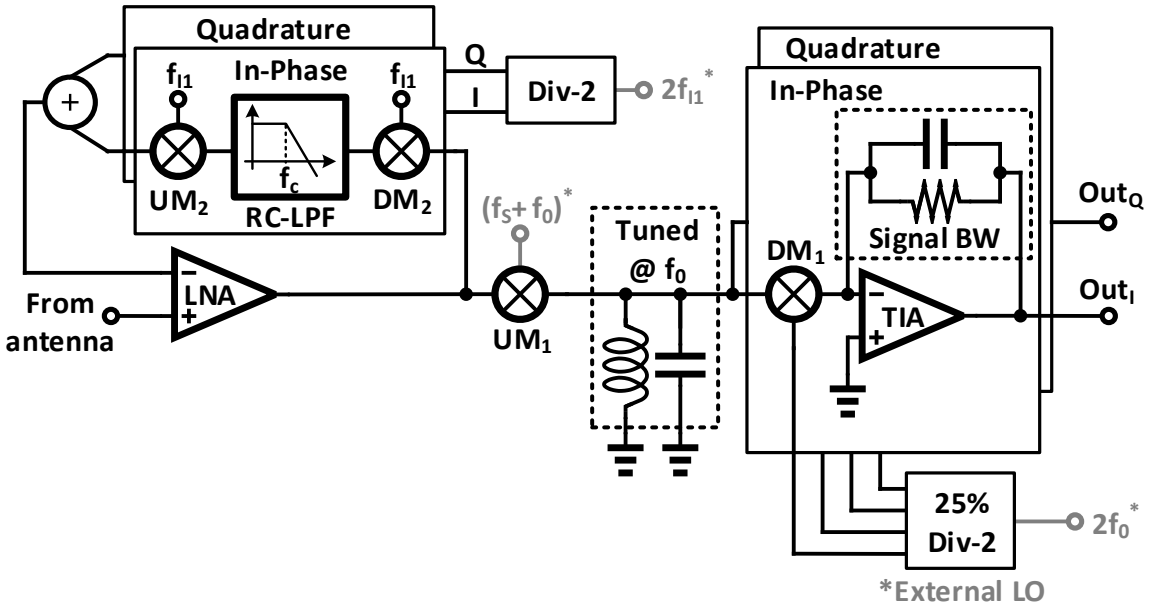


Figure 2.8: Block diagram of the complete receiver. The receiver is shown in single-ended fashion for simplicity. The LO signals are provided externally.

2.5.1 LNA

Fig. 2.9 shows the fully-differential dual-input LNA, implemented in the receiver. The special architecture of the LNA is mandated by the fact that the LNA is incorporated into the active feedback loop. As can be seen from Fig. 2.6, the output of the loop, ie output of the UM_2, which is fed to the negative input port of the LNA is a differential signal. It requires the LNA to have a double-differential input. A differential to single-ended converter might be used at the interface of the loop and the LNA to eliminate this requirement, but this is hard to achieve without further degrading the NF.

The LNA is basically comprised of two differential pair ($\mathrm{M}_{1,2}, \mathrm{M}_{3,4}$), connected together at their outputs. A CG amplifier ($\mathrm{M}_{5,6}$) is also providing wideband input matching for the positive port, connected to the antenna. Transistors M_5 and M_1 (or M_6 and M_3) form a noise canceling CG/CS structure [51], so that by proper biasing of the differential pair, noise of M_5 (and M_6) can be canceled at the output.

To further increase the blocker tolerance of the LNA, a 5 pF capacitor C_g is ac-coupling the gates of M_5 and M_6 to the output of the loop ($\mathrm{IN}_{\mathrm{n}+}, \mathrm{IN}_{\mathrm{n}-}$). By doing so, $\mathrm{V}_{\mathrm{GS}_{5,6}}$ is not affected by the large common-mode swing of the blocker which is appearing on the $\mathrm{IN}_{\mathrm{p}+}$ and $\mathrm{IN}_{\mathrm{n}+}$, in one side and, $\mathrm{IN}_{\mathrm{p}-}$ and $\mathrm{IN}_{\mathrm{n}-}$, on the other side. The Common-Mode Rejection Ratio (CMRR) of the LNA plays a key role for this design to work properly. As was shown in Fig. 2.5, ideally the interferer is supposed to be attenuated by the loop gain, however this attenuation becomes limited to the CMRR, if it is smaller than the loop gain. Common-mode gain in a differential amplifier stems from the limited output impedance of the tail current sources. This phenomenon is mitigated in the LNA in two ways; first, the common-mode currents generated through modulating the output of the differential pairs tail current sources are canceled at the output[9], and second, since there is

[9]The drain current of M_1 cancels that of M_4, and M_2 that of M_3.

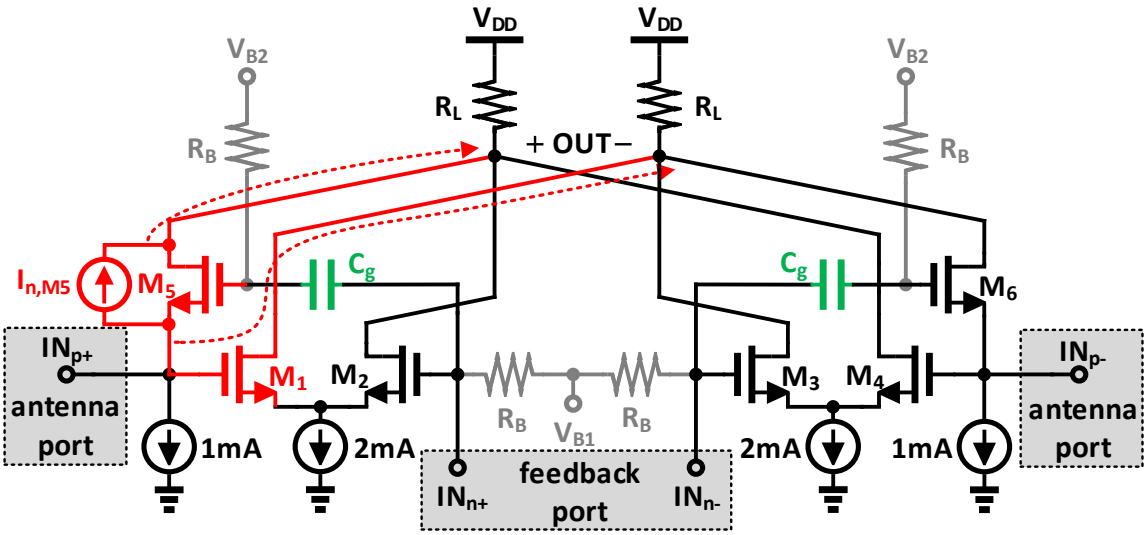


Figure 2.9: The fully-differential, dual-input LNA. Noise canceling paths are shown in red. Note that the LNA has two differential input ports $\mathrm{IN_p}$, and $\mathrm{IN_n}$, and the common-mode signals appear on the input in a way that $\mathrm{IN_{p+}}$ is in-phase with $\mathrm{IN_{n+}}$, and $\mathrm{IN_{p-}}$ with $\mathrm{IN_{n-}}$.

enough voltage headroom left for the 1 mA current source transistor ($\mathrm{V_{GS_{1,4}}} + \mathrm{V_{OD_{2mA}}}$), cascoding it increases its output impedance significantly.

Fig. 2.10 illustrates the gain, NF, CMRR, and input matching of the LNA across the entire CR band. The LNA consumes 6.5 mA and has a DC gain of around 16.2 dB[10], with a 3-dB point bandwidth (considering the loading effect of the following blocks) of around 1.85 GHz. CMRR of the LNA is also simulated to be more than 30 dB over the CR band which is larger than the active feedback loop gain. The simulations show $\mathrm{IIP_3}$ of more than 7 dBm over the entire band for the LNA. The special structure of the LNA limits the gain strictly. The voltage headroom is divided between $\mathrm{R_L}$, $\mathrm{V_{GS_{5,6}}}$, $\mathrm{V_{GS_{1,4}}}$, and overdrive voltage of the 2 mA tail bias current. As a result the voltage headroom for $\mathrm{R_L}$ and consequently the gain is limited.

[10]Note that this is the gain seen from the input single-ended source to the differential output of the LNA, so it includes 3 dB passive gain of the input differential splitter. The gain seen from the differential input of the LNA to the output is 13.2 dB.

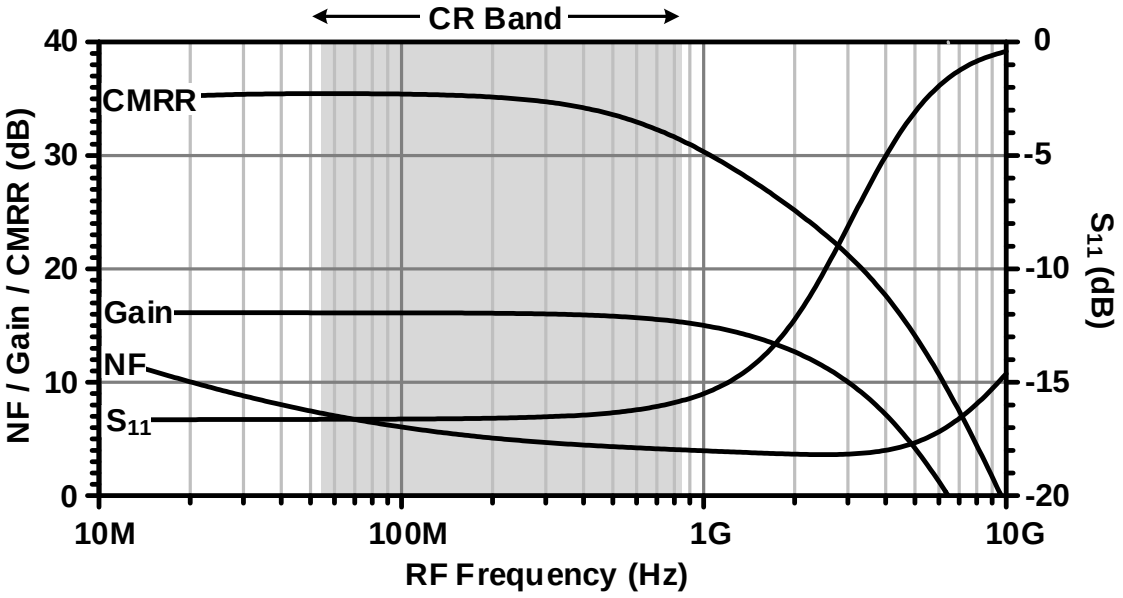


Figure 2.10: Simulated Gain, NF, CMRR, and input matching of the LNA.

2.5.2 Active Feedback Path

The active feedback path (Fig. 2.11(a)), as discussed previously, is comprised of a down-conversion mixer (DM_2), a single-pole RC low-pass filter (LPF), and an up-conversion mixer (UM_2). To relax the gain-linearity trade-off of the mixers, a pseudo-differential RF stage structure is used (Fig. 2.11(b)). Besides the fact that a pseudo differential architecture is inherently more linear, larger overdrive voltage can be allocated to the RF stage transistors to enhance the linearity of the mixers. However, there are two problems with this approach; first, the common-mode output voltage of DM_2 is not in a suitable range for the next NMOS stage to work, and second, setting the bias current of the RF stage transistors of UM_2 depends on the output voltage of DM_2, which can vary significantly, mainly due to variation of the DM_2 load resistors. To address these issues DM_2 is followed by a low-gain amplifier acting as a level-shifter buffer as shown in Fig. 2.11(c). In this case, the output common-mode voltage of the amplifier is set through a feedback loop, making

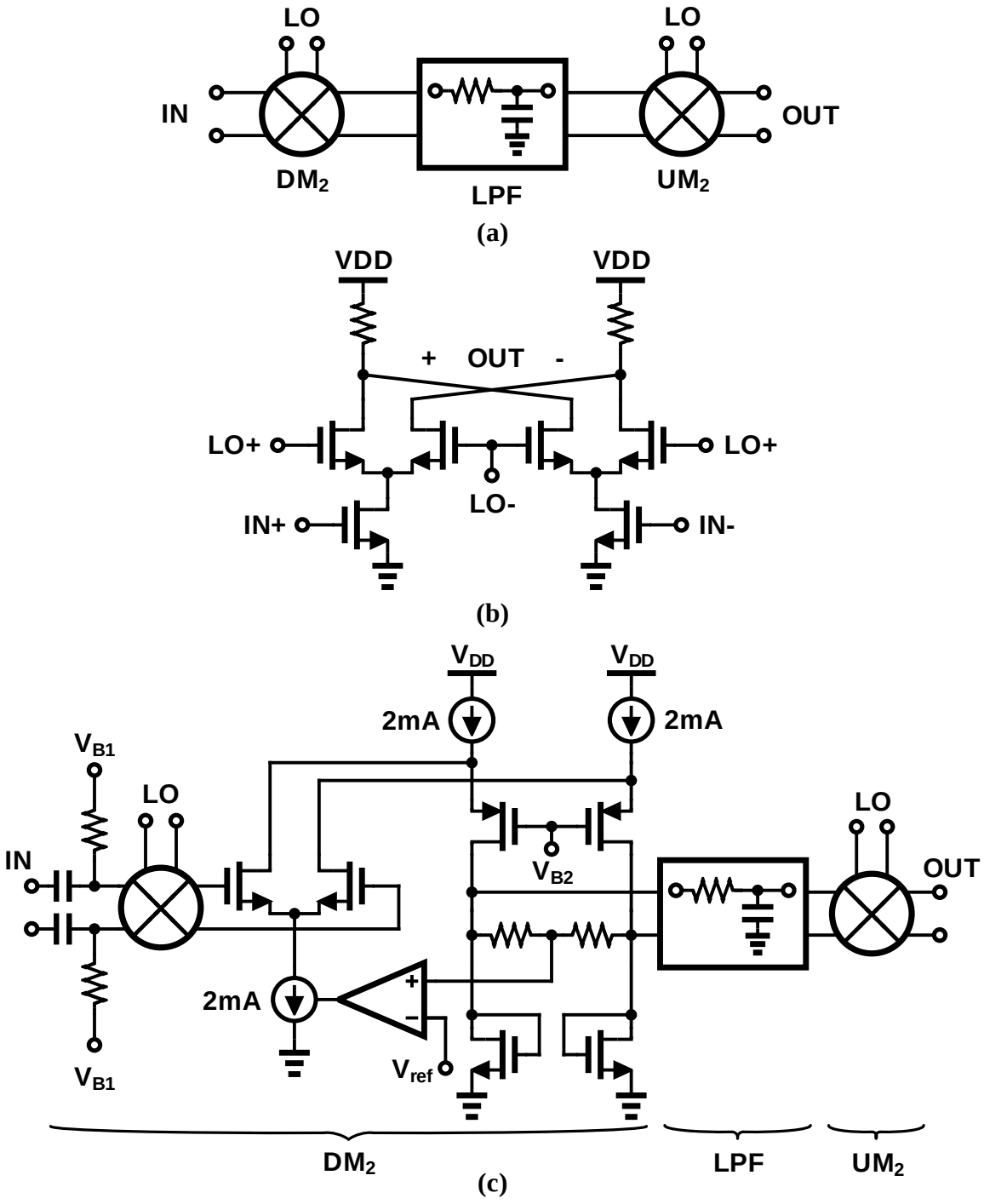


Figure 2.11: (a) Simple active feedback path. (b) Pseudo-differential double balanced mixer architecture, used to realize DM_2 and UM_2. (c) Final active feedback path. Note that the bias condition of UM_2 RF stage is set through the common-mode feedback of the amplifier.

it resilient toward process variations, and providing a proper bias condition for the next NMOS stage. The diode connected transistors not only provide process variation resilient bias voltage for $\mathrm{UM_2}$, but also provide a linear gain for the amplifier. Note that $\mathrm{DM_2}$, unlike $\mathrm{UM_2}$, can be ac-coupled to its preceding stage, since the incoming signal is located at RF frequencies whereas the $\mathrm{UM_2}$ input signal is located around DC. It is worth mentioning that, LPF also filters out the noise at the desired signal frequency, therefore the excess noise of this amplifier does not affect the overall performance of the receiver noticeably. $\mathrm{DM_2}$ combined with the amplifier consumes 5 mA, and provides around 6 dB of gain, and has an $\mathrm{IIP_3}$ of about +2 dBm. Also, simulations show an $\mathrm{IIP_3}$ of around +6 dBm and a conversion gain of 9 dB for $\mathrm{UM_2}$ while drawing 4 mA from supply.

The LPF introduces the dominant pole of the loop with 90 degree phase shift. The excess phase shift, caused by other blocks in the loop therefore determines the stability and phase margin of the loop. Fig. 2.12 shows the loop gain and phase for the case when the loop is working at 450 MHz, and $\mathrm{f_c}$ = 500 kHz. The phase margin in this case is around 54 degree. In fact, phase margin drops from around 75 degree, for the lowest boundary of the CR band (i.e. 50 MHz) to the minimum of 31 degree for the highest boundary of the CR band (i.e. 850 MHz). Different process corners and temperature can affect the stability of the loop. In fact in the worst case scenario of $\mathrm{f_{I1}}$ = 850 MHz, SS corner, and temp = 75°, the phase margin drops to less than 10°. To improve the phase margin $\mathrm{f_c}$ can be lowered, limiting the bandwidth of interferer rejection, or in a better solution, smaller feature size with less parasitics CMOS technologies can be used.

The phase and gain imbalance of the quadrature active feedback path are of concern for two reasons:

1. As shown in [44], I/Q phase and gain mismatch can reduce the loop gain and phase margin. The maximum possible deterioration of loop gain and phase margin for

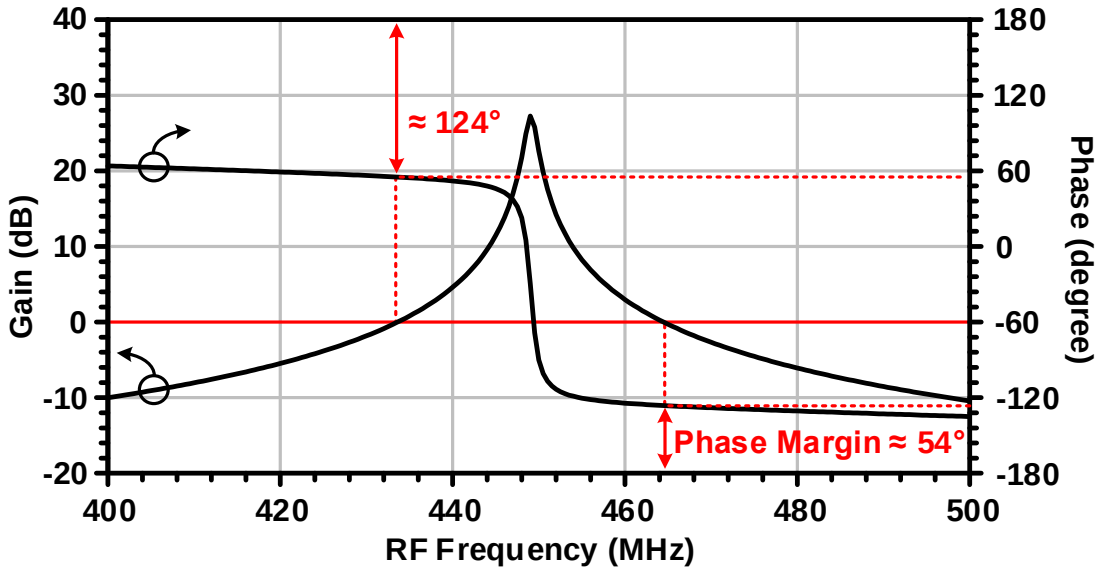


Figure 2.12: Loop gain and phase of the active feedback loop, when the loop is working at $f_{I1} = 450$ MHz. Phase margin and unity gain bandwidth of the loop are simulated to be around 54 degree and 30 MHz, respectively.

$-10° < \epsilon_\Phi < 10°$, and $-5\% < \epsilon_G < 5\%$ are 1.8 dB and 10°, and 0.46 dB and 5° respectively, where ϵ_Φ, and ϵ_G are I/Q phase and gain imbalance.

2. An attenuated replica of the second interferer appears at the frequency of the desired signal, i.e. f_S, at the output of the feedback path[11]. This attenuation can be estimated by

$$\frac{\epsilon_\Phi}{2}\frac{1}{\sqrt{1+\left(\frac{\Delta f}{f_c}\right)^2}} \tag{2.13a}$$

$$\frac{\epsilon_G}{4}\frac{1}{\sqrt{1+\left(\frac{\Delta f}{f_c}\right)^2}} \tag{2.13b}$$

where the second term in (2.13a) and (2.13b) is the attenuation introduced by the

[11] It would ideally up-convert back to its original frequency, i.e. f_{I2}.

LPF. Given the same constraints as before for ϵ_{Φ}, and ϵ_{G}, and two interferers with 50 MHz offset frequency, the replicated interferer becomes attenuated at least as much as 61.6, and 78 dB, respectively.

It is worth noting that the active feedback path I/Q LO signal phase noise does not degrade the NF of the receiver as it is located far from the desired signal.

2.5.3 Heterodyne Conversion; $\mathrm{UM_1}$, $\mathrm{DM_1}$, and TIA

Fig. 2.13 illustrates the heterodyne conversion part of the receiver, consisting of a pseudo differential Gilbert cell up-converting mixer $\mathrm{UM_1}$, and passive current driven down-conversion mixer $\mathrm{DM_1}$ followed by a TIA. The pseudo differential pair of $\mathrm{UM_1}$ is biased at $\mathrm{I_D}$ = 2 mA. Simulation shows an $\mathrm{IIP_3}$ of 13.5 dBm for the $\mathrm{UM_1}$ stand alone. Since the passive mixer stage $\mathrm{DM_1}$ is transparent, the load of $\mathrm{UM_1}$ becomes nonlinear, therefore to prevent from nonlinearity of the following stages affecting the simulation, the nonlinearity of $\mathrm{UM_1}$ is measured through its output current when the output is ac ground. Note that the nonlinearity of a pseudo differential Gilbert mixer is mainly caused by the nonlinearity of its RF stage transistors ($\mathrm{M_{1,2}}$ in Fig. 2.13) and manifests itself in drain current of $\mathrm{M_{1,2}}$, particularly if the output swing and the biasing of the LO stage is in a way that the switching transistors do not experience triode region during the signal excursion. Low input impedance of $\mathrm{DM_1}$, employing an inductive load, and pseudo differential architecture of $\mathrm{UM_1}$ leave enough headroom to ensure that the nonlinearity of $\mathrm{UM_1}$ is dominated by $\mathrm{M_{1,2}}$, and the simulation result is reasonably correct.

According to [50], and [52], to achieve the maximum linearity and conversion gain for the passive mixer, $\mathrm{L_0}$ should resonate with $\mathrm{C_0 + 2C_s}$ at ω_{RF}. On the other hand, $\mathrm{C_s}$ must have an impedance with a magnitude $\mathrm{X_{C_s}} = \sqrt{2\mathrm{R_0}(\mathrm{R_{SW}} + (1/\pi^2)\mathrm{R_{BB}})}$, where $\mathrm{R_{SW}}$ and $\mathrm{R_{BB}}$ ($\mathrm{Z_{BB}}$) are the ON resistance of the passive mixer switches, and impedance seen from the input of the TIA, respectively. An inductor with differential inductance of 8.5 nH and

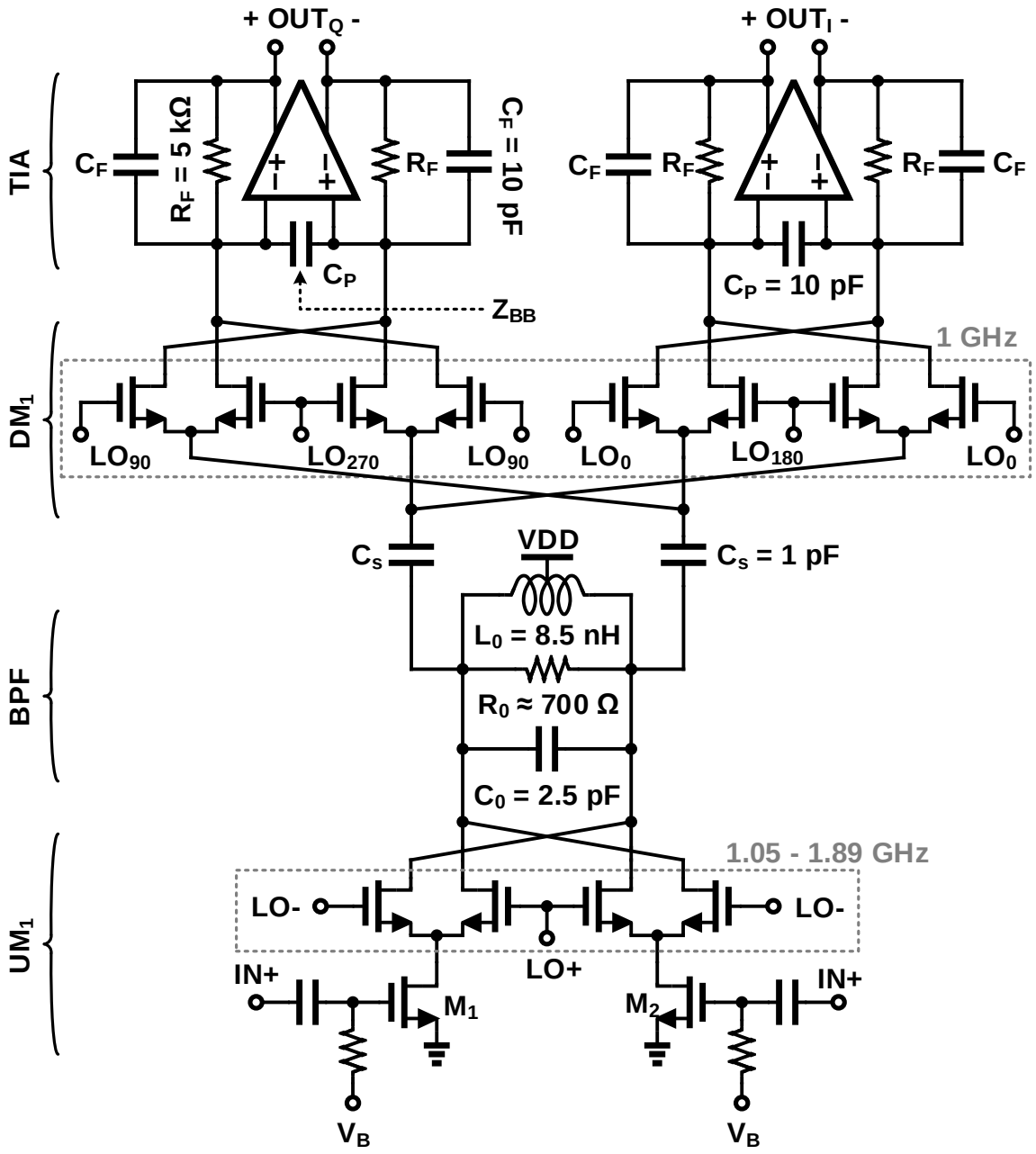


Figure 2.13: The schematic of the heterodyne conversion block.

quality factor of 10.5 ($\mathrm{R}_0 = 700\ \Omega$) is selected. Considering the bias condition, switches are sized for an ON resistance of $\mathrm{R}_{\mathrm{SW}} = 13\ \Omega$. Therefore, C_s, and C_0 found to be 1 and 2.5 pF, respectively.

Also as shown in [53], the passive mixer load impedance (Z_{BB}) plays a major role on its linearity; lower impedance results in lower voltage swing and higher linearity. Therefore a lower R_F is suitable to achieve higher IIP_3, whereas a larger R_F provides more conversion gain. The IIP_3 degradation would be more significant for interferers at higher offset frequencies, where the loop gain of the TIA drops and the passive mixer experiences larger Z_{BB}. One way to address the latter issue is to increase C_F, so that the load impedance seen by the passive mixer at higher offset frequencies decreases. Increasing C_F alone cannot solve the problem, first because it limits the bandwidth of the receiving signal, and second, at high enough frequencies Z_{BB} increases and peaks, regardless of C_F. To overcome this problem, a parallel capacitor C_P can be added to the input of the TIA [34]. In this way the bandwidth of the receiver is not affected by C_P, while at high frequencies, the peak impedance of Z_{BB} drops significantly, consequently improving IIP_3 at high offset frequencies.

As shown in Fig. 2.14, a two stage TIA is designed with DC gain of 58 dB, while consuming 6.5 mA. Note that stability of the TIA is influenced by its RC feedback network, therefore there are three constraints to pick R_F, C_F, and C_P; first, to set the receiver bandwidth of 6 MHz we should have $\frac{1}{2\pi C_F R_F} = 3\ \mathrm{MHz}$, second, among all the possible combinations of R_F, and C_F, those should be selected that provide lower load impedance for DM_1, and third, result in higher unity gain bandwidth (UGB) product and phase margin for the TIA.

Z_{BB} is depicted for different choices of R_F, C_F, and C_P versus baseband (BB) frequency in Fig. 2.15. It can be seen that each of R_F, C_F, and C_P dominates Z_{BB} at certain range of frequencies. At very low frequencies (below 1 MHz), R_F is the dominant factor. C_F is more predominant at mid range frequencies ($5 \sim 50$ MHz), and the effect of C_P is visible only at high frequencies (above 100 MHz).

Fig. 2.15 might seem to suggest larger C_F, and C_P provide lower input impedance

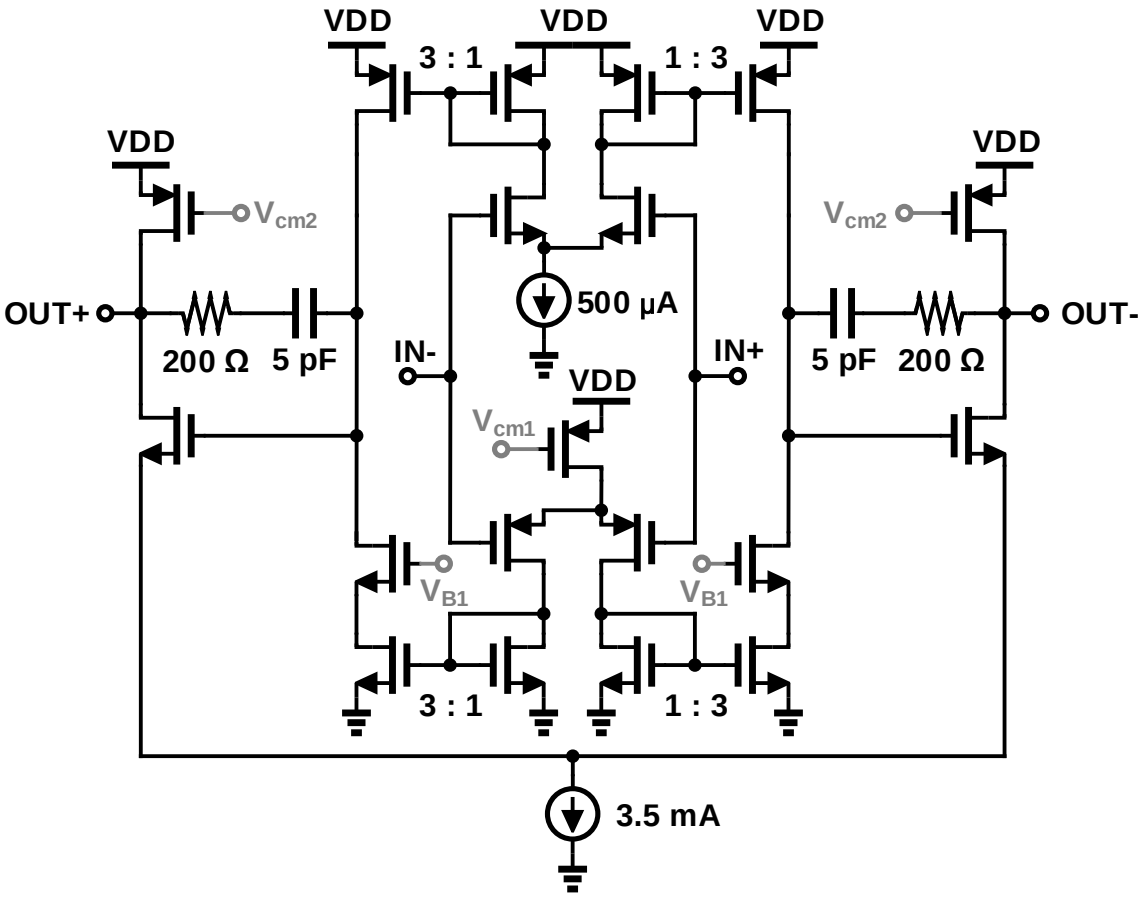


Figure 2.14: The schematic of the fully-differential 2-stage TIA.

and therefore better linearity, but Fig. 2.16 shows that selecting very large values for $\mathrm{C_F}$, and $\mathrm{C_P}$ results in low phase margin and risk of TIA instability, or lower UGB for the TIA, respectively. Ultimately, $\mathrm{R_F} = 5\ \mathrm{k\Omega}$, $\mathrm{C_F} = 10\ \mathrm{pF}$, and $\mathrm{C_P} = 10\ \mathrm{pF}$ are selected that result in UGB of 300 MHz and phase margin of 54 degree.

Fig. 2.17 illustrates the IIP3 of the Heterodyne-Conversion (HC) block, for various $\mathrm{R_F}$, $\mathrm{C_F}$, and $\mathrm{C_P}$ choices versus baseband frequency. The counter-intuitive observation from Fig. 2.17 is that increasing $\mathrm{R_F}$ improves IIP3, while it was expected to degrade IIP3 by increasing $\mathrm{Z_{BB}}$. However, considering Fig. 2.15, it is clear that at frequencies above $\sim$ 3 MHz, $\mathrm{R_F}$ virtually has no effect on $\mathrm{Z_{BB}}$ and it is $\mathrm{C_F}$ and $\mathrm{C_P}$ that determine $\mathrm{Z_{BB}}$.

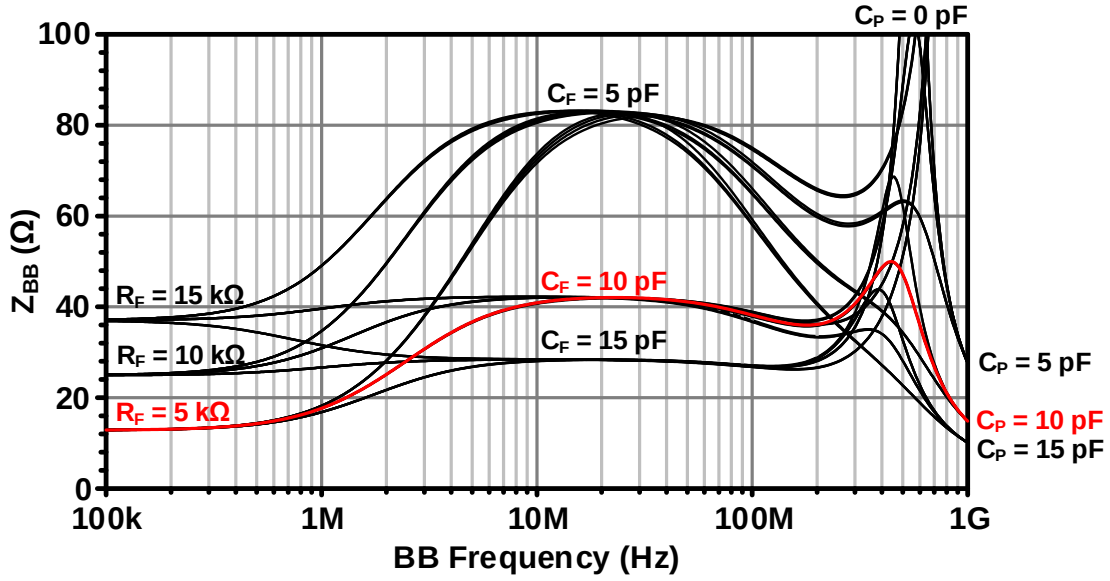


Figure 2.15: Baseband impedance Z_{BB} seen from the output of DM_1 Vs. baseband frequency for different choices of R_F, C_F, and C_P.

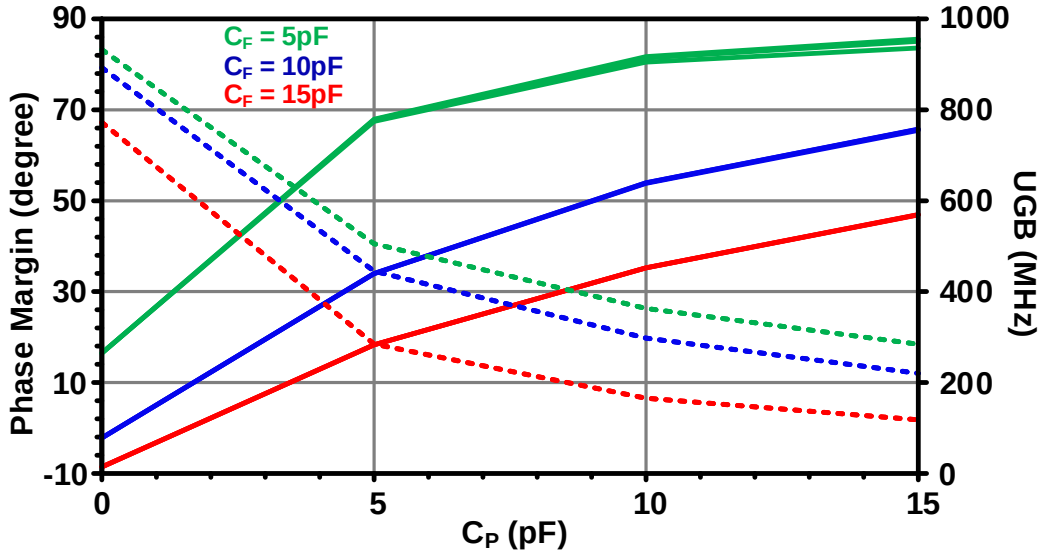


Figure 2.16: Phase margin (solid), and UGB (dotted) of the TIA for different values of R_F, C_F, and C_P. Note that varying R_F from 5 to 15 kΩ almost has no noticeable effect on the stability performance of the TIA.

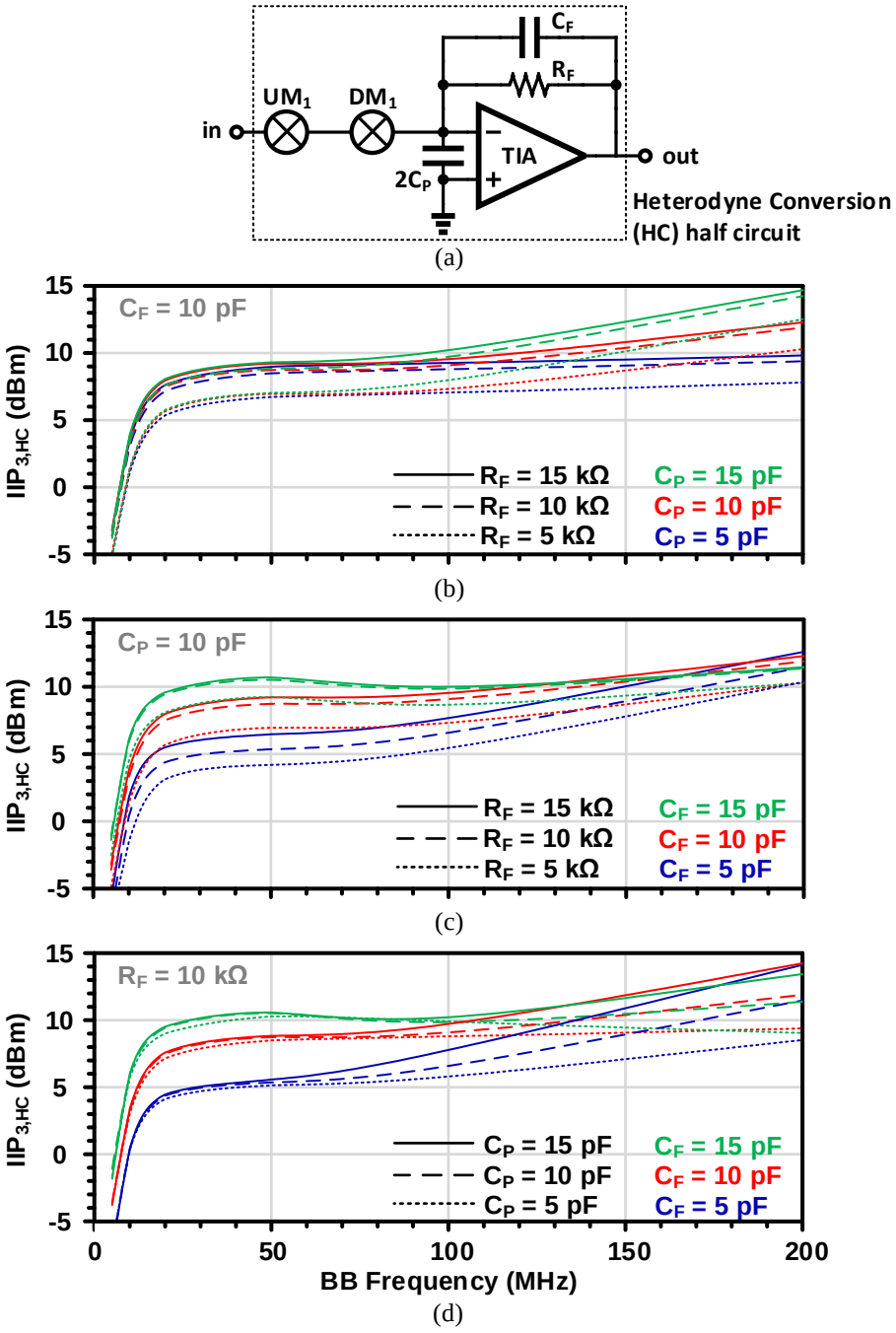


Figure 2.17: (a) Half circuit of the simulated Heterodyne-Conversion (HC) block. (b-d) Simulated IIP3 of HC block for different choices of R_F, C_F, and C_P vs. baseband frequency.

Therefore by increasing $\mathrm{R_F}$ for interferers at distant offset frequencies (above $\sim$ 3 MHz), γ_3, which models the nonlinearity effect of HC block, is unaffected. At the same time γ_1, which models the small signal gain of HC block at very low offset frequencies (below $\sim$ 3 MHz) and depends on $|\mathrm{Z_{BB}}|$ increases. Therefore by increasing $\mathrm{R_F}$, at high offset frequencies, $\mathrm{IIP_{3,HC}} \propto \sqrt{|\frac{\gamma_1}{\gamma_3}|}$ increases. On the other hand, at low frequencies, increasing $\mathrm{R_F}$, increases $|\mathrm{Z_{BB}}|$, and with the same token, it would degrade the in-band IIP3.

2.5.4 LO Generation

The LO signals in this design are provided externally. A Current Mode Logic (CML) divider-by-2 accepts differential LO signal from 100 MHz to 1.7 GHz, and generates required quadrature clocks from 50 to 850 MHz for $\mathrm{DM_2}$, and $\mathrm{UM_2}$ in the active feedback path. The divider-by-2 and the buffers driving these mixers consume 5.5 and 2.6 mA at the higher and lower end of the frequency band, respectively. Another divider-by-2 similar to that in [34] receives a 2 GHz differential clock and generates four 25% duty cycle clocks at half the frequency (i.e. 1 GHz) that drives $\mathrm{DM_1}$, while consuming around 6 mA.

2.6 Measurements

Fig. 2.18 shows the chip photo of the receiver implemented in 180 nm CMOS technology. It occupies 1.16×2 mm^2. The receiver operates from 50 to 850 MHz. Three different LO signals are provided externally; two of which are driving heterodyne conversion mixers UM_1 and DM_1 as described in Fig. 2.8, and the other one drives feedback loop mixers UM_2 and DM_2. The I/Q signals are generated internally. Two different operational modes are defined for the receiver: 1) Interferer-Free mode, in which the active feedback loop is off; this is the case when there is no destructive interferer along with the desired signal, and 2) Interferer-Tolerant mode in which the active feedback loop is on; this is the case when the desired signal is disrupted by the presence of interferers.

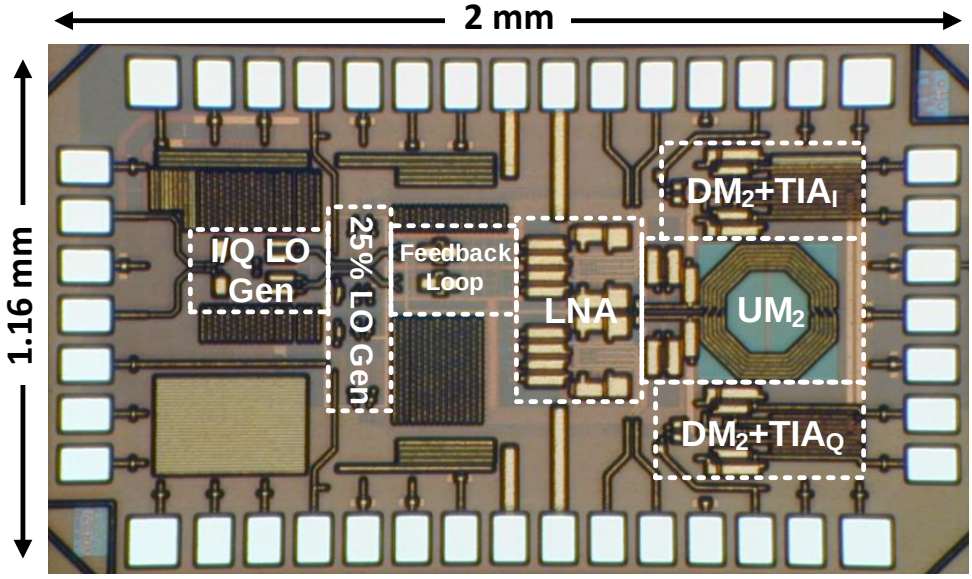


Figure 2.18: Chip micro-photograph fabricated in 180 nm CMOS.

The receiver draws about 25 and 40 mA current from a 1.8 V supply in the interferer-

Table 2.2: Power Breakdown of the Receiver

LNA	6.5 mA	TIA	6.5 mA
$\mathrm{UM_2}$	4 mA	$\mathrm{DM_2}$ + Amp	5 mA
$\mathrm{UM_1}$	4 mA	Div-2 (2 GHz)	6 mA
Div-2 (0.1-1.7 GHz)	2.4-3.5 mA	LO Buffer (50-850 MHz)	20-250 uA

free and interferer-tolerant modes[12], respectively. The power breakdown of the receiver is presented in Table 2.2.

Fig. 2.19 depicts the measured $\mathrm{S_{11}}$ curves for two different configurations; black lines represent the interferer-tolerant mode where the active feedback loop frequency ($\mathrm{f_{I1}}$) is varied from 100 to 700 MHz with 200 MHz steps, and red line represent the input matching for the interferer-free mode in which the active feedback loop is off. In the interferer-tolerant mode, since the negative feedback is closed at $\mathrm{f_{I1}}$, the input impedance seen at this frequency increases, and by diverging from the active loop frequency, where the loop gain drops, the input impedance converges to that of interferer-free mode.

Fig. 2.20 shows the simulated and measured receiver small signal NF versus RF frequency, i.e. the desired signal channel frequency. Fig. 2.20 plots effective NF, i.e. average NF over the 3 MHz baseband bandwidth, since due to flicker noise, NF increases at low offset frequencies. The NF in the interferer-free mode (when the active feedback loop is off) is shown at the bottom; at the lower end of the band, due to flicker noise of the LNA (as can be seen in Fig. 2.10) NF is about 9 dB and reduces to a minimum of about 7.5 dB for the most part of the band. It is still however at least 1.5 dB higher than the standard suggestion. In the interferer-tolerant mode, when the active feedback loop is on, the NF increases as was expected. NF in this case also is affected by the active feedback loop frequency, or in other words the offset frequency ($\Delta\mathrm{f}$) between the desired signal and the

[12]The LO buffers and dividers are excluded, while consuming 6.5 and 11.5 mA in each mode, respectively.

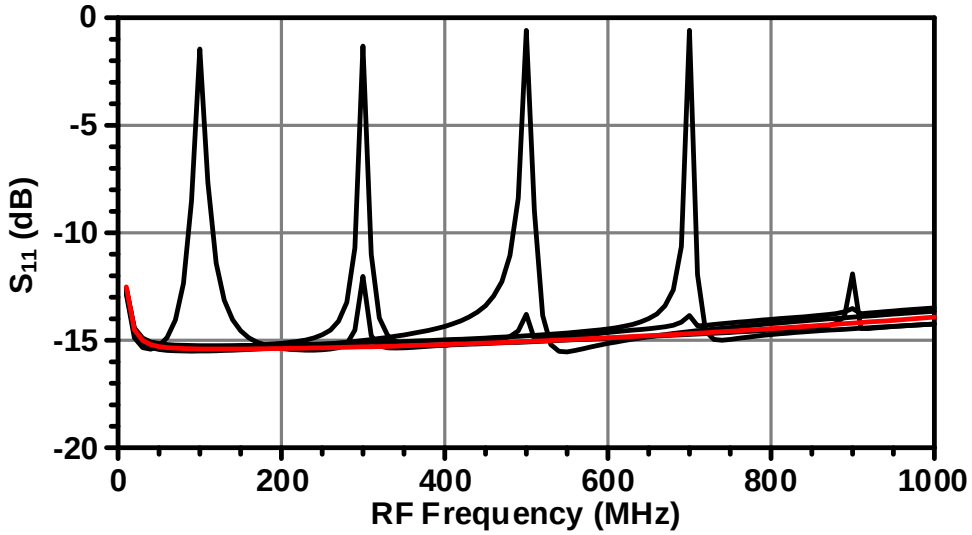


Figure 2.19: The measured input matching of the receiver in interferer-tolerant (black), and interferer-free (red) mode where the active feedback loop is on and off, respectively.

interferer. At low offset frequencies NF rises more for two reasons; first, the up-converted flicker noise of UM_2 (Fig. 2.7) starts to manifest itself, and second, at very low offset frequencies (lower than 50 MHz) the LPF attenuates the signal less and therefore the gain of the receiver starts to drop as can be seen from (A.4) in the Appendix. However at high offset frequencies the difference in NF is negligible. Fig. 2.20 shows the NF in the interferer-tolerant mode for four different offset frequencies over the receiving band, and depending on the desired signal and the active feedback frequency varies between 14.7 to 10.5 dB.

A strong interfere desensitizes the receiver by increasing its NF; it causes the gain of the receiver to drop through gain compression, while the output noise stays almost unchanged, resulting in higher NF and less sensitivity. Employing the active feedback to reject this strong interferer can keep the gain of the receiver unaffected for stronger interferers, and therefore keep the NF from rising. Fig. 2.21 depicts the NF and normalized gain of the receiver, when there is a strong interferer at f_{I1}= 200 MHz along with the desired

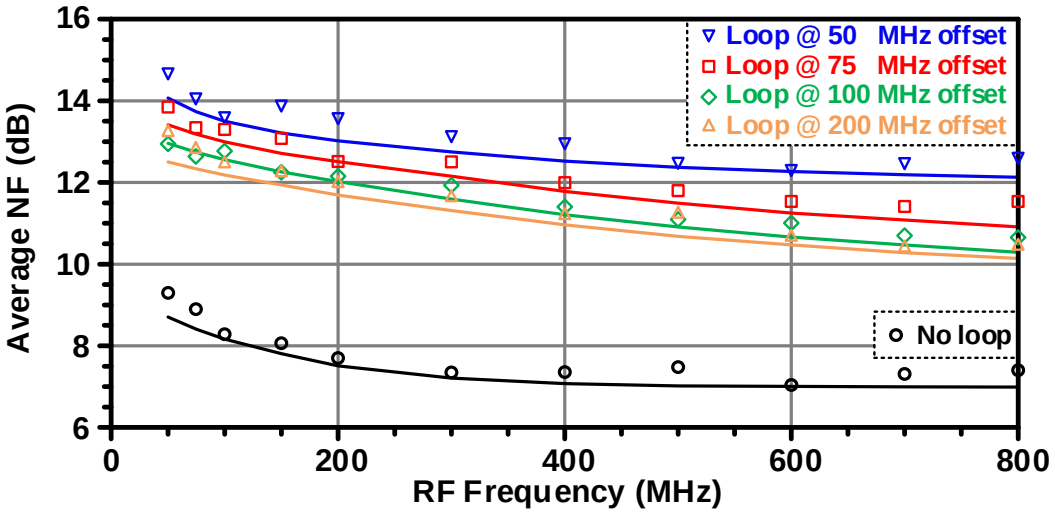


Figure 2.20: Small signal NF vs. RF frequency, i.e. desired signal frequency f_S. NF in interferer-free mode is shown at the bottom. NF in interferer-tolerant mode is depicted for four cases; where the feedback loop is working at $\Delta f = |f_S - f_{I1}|$= 50, 75, 100, and 200 MHz offset from the desired signal. Solid lines depict simulation results.

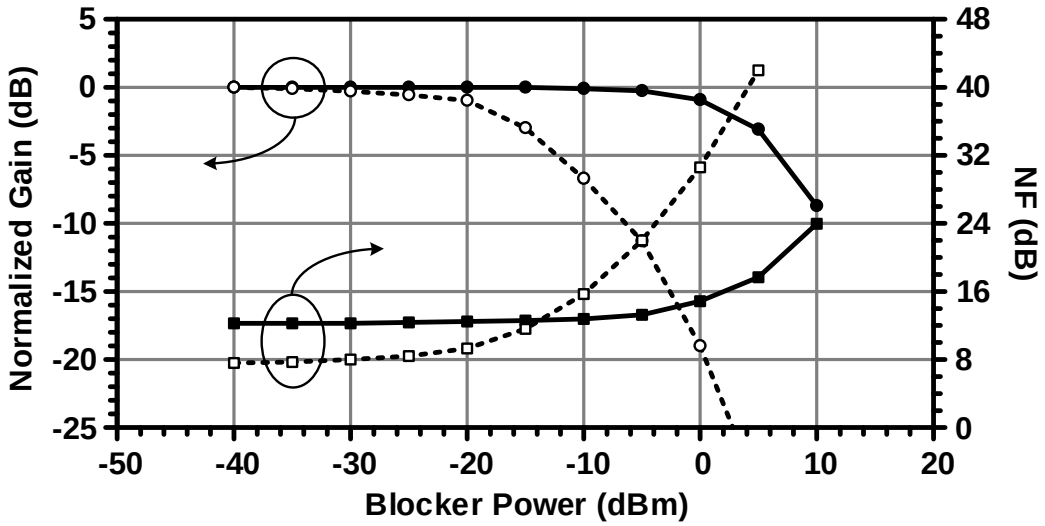


Figure 2.21: Measured blocker NF and and normalized gain of the receiver vs. blocker power for interferer-tolerant (solid) and interferer-free (dotted) modes. The blocker and signal are applied at $f_I = 200$ MHz, and $f_S = 300$ MHz.

signal at f_S= 300 MHz, in two cases. Although in the interferer-tolerant mode, in which the feedback loop is active, the NF is inherently suffering from the excess noise of the loop, the NF surpasses that of interferer-free mode for interferers stronger than -15 dBm.

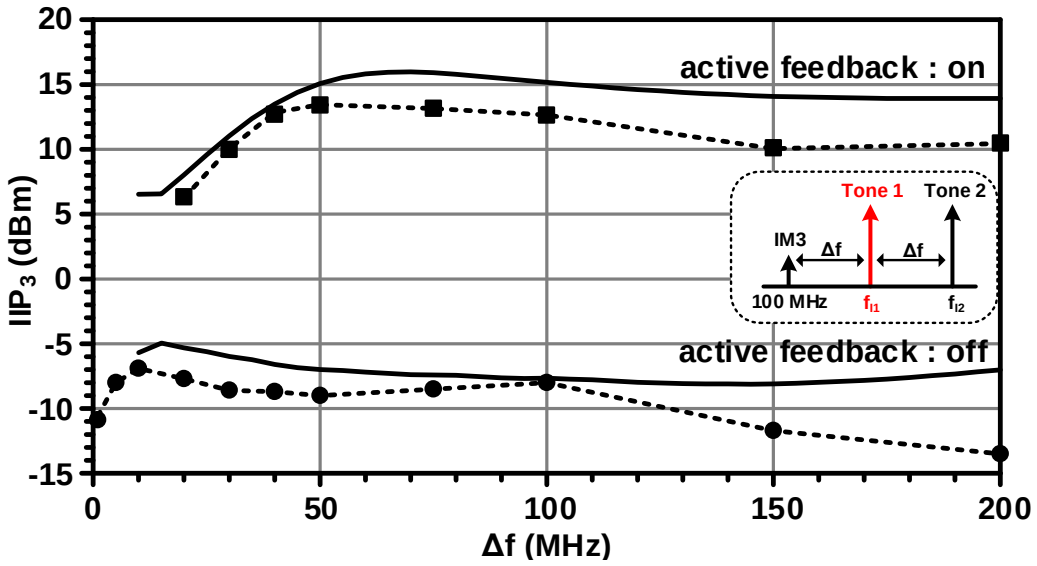


Figure 2.22: Simulated (solid) and measured (dotted) $\mathrm{IIP_3}$ of the shown two-tone test scenario. The active feedback loop, improves $\mathrm{IIP_3}$ (or in other word rejects the interferer) by around 20 dB. The active feedback loop is set to select Tone 1 in all cases. The dotted line shows measurement results.

The $\mathrm{IIP_3}$ is measured using two tones at f_{I1} and f_{I2} and the scenario that is depicted in Fig. 2.22. The lines on the bottom show the $\mathrm{IIP_3}$ for the interferer-free mode where the in-band $\mathrm{IIP_3}$ is about -11 dBm and OB-$\mathrm{IIP_3}$ varies from -7 to -14 dBm. By bringing on the active feedback loop that is set at f_{I1}, the receiver can block and filter out the interferer located at this frequency. As explained in Section 2.4.1, this can be quantified in terms of $\mathrm{IIP_3}$. The solid line on top shows the simulated $\mathrm{IIP_3}$ for the particular scenario that is described in the figure, while the dotted line shows the measurement results. Table 2.3, presents different scenarios by which IIP2 is measured. Due to the vast bandwidth of the

CR band and possibility of various scenarios, it is difficult to set up a unified scenario to measure IIP2, unlike the case for IIP_3.

Table 2.3: Measured IIP2 in Different Scenarios with and without Active Feedback Loop.

f_{I1} (MHz)	f_{I2}[1] (MHz)	f_S 300 (MHz)	IIP2 (dBm)	
			IF[2]	IT[3]
460	760	$f_{I2} - f_{I1}$	39.3	57.5
240	540	$f_{I2} - f_{I1}$	47.7	61.2
120	180	$f_{I2} + f_{I1}$	56.2	70.9
80	220	$f_{I2} + f_{I1}$	38.7	55.1

[1] f_{I2} is offset by 250 kHz.
[2] Interferer-Free mode.
[3] Interferer-Tolerant mode. Active loop is working at f_{I1}.

2.7 Discussion

Table 2.4 compares this work with the recently published state-of-the-art wideband CMOS receivers. As can be seen from the table, poor NF is the major downside of the active feedback technique. Smaller feature size CMOS technologies enable employing active load for the LNA, and by improving its gain, can improve NF, particularly the part that is contributed by heterodyne-conversion block. Since in the interferer-tolerant mode, the feedback path noise is a significant contributing factor to NF, using passive mixers, as in [45], can improve NF in this mode too. However, since passive mixer input impedance varies with the LO frequency, the loop parameters is subject to drastic variations for wide-band applications, therefore maintaining desired loop parameters requires additional circuitry. It is also worth noting that although [30] has achieved an excellent IIP_3 of +25 dBm at low offset frequency of 25 MHz, it has been achieved by compromising the signal bandwidth[13], and area, as it needs to engage as much as sixteen 120 pF load capacitors. Moreover, [34], and [36] use noise cancellation technique to achieve an outstanding NF of less than 2 dB. However, in order to maintain this NF, a very low-noise LO signal is required which translates into higher power consuming VCO [36].

The nonlinearity, as discussed in this paper, can affect the performance of the receiver in various fashions, however the two major cases are, when a very strong interferer appears at the input and causes the gain to compress and NF to increase and, when two or more out-of-band interferers appear on the spectrum in a way that their intermodulation products coincide with the desired signal. Although it is fairly reasonable to assume in the vastly broadband spectrum of the CR, there can be numerous interferers, it is not likely to have a situation in which all of the interferers result in an IM3 component that is located at the same location. In other words, assuming two interferers create a destructive IM3

[13]The exact bandwidth is not reported.

Table 2.4: Measurement Summary and State-of-the-Art Comparison

Ref.	Unit	[28]	[30]	[34]	[36]	[38]	[45]	[46]	[54]	This Work
Frequency	GHz	0.4-6	0.1-2.4	0.1-2.8	0.08-2.7	0.4-0.9	1-2.5	0.05-0.86	0.05-6	0.05-0.85
Freq. Conversion		Direct	Direct	Direct	Direct	Direct	Direct	Direct	Heterodyne	Heterodyne
Gain	dB	70	40-70	50	72	34	30	0-100	-24-88	54
OB-IIP_3	dBm	+10	+25	+5	+13.5	+16	+12	N/A	-6	+13
@ $\Delta f = f_I$ - f_S	MHz	20	25	50	20	800	60		100	50
IB-IIP_3	dBm	+6	-67	-15	N/A	+3.5	-20	-29.6	-11	-11
IIP2	dBm	+70	+56	+50	+55	+56	>+49	N/A	>+60	>+55
NF	dB	3-8.25	3-5	1.8	1.9	4	7.25-8.9	3.5-7	3.8-10.7	7.5-13[1]
Blocker NF	dB	13		14	4.1				22.5	15.5
@ $P_{Blocker}$	dBm	0	N/A	0	0	N/A	N/A	N/A	0	0
@ $\Delta f = f_I$ - f_S	MHz	20		50	80				80	50
$3^{rd}/5^{th}$ HR	dBc	N/A	35/46	N/A	42/45	60/64	N/A	43/56	75	>70[2]
Area	mm^2	2	2.5	0.8	1.2	1	<0.06[3]	12.2[4]	52.8[4]	2.3
Supply	V	1.1/2.5	1.2/2.5	1.1	1.3	1.2	1.2	1.8	1.5/2.5	1.8
Power	mW	30-55	37-70	27-40	35-78	60	62	83-112	720-890[4]	45-72
Technology	nm	40	65	40	40	65	65	180	130	180

[1]Interferer-free/tolerant mode at midband (ie. 400 MHz).
[2]For all the harmonics. Assuming 40 dB rejection beyond 2 GHz for the input filter.
[3]Active area.
[4]Complete transceiver, including LO generation.

component (coinciding with the desired signal), it is very unlikely to have a third interferer located in a way that creates an IM3 component (in conjunction with the first two interferers) at the same location[14] (i.e. the desired signal frequency). However if the number of interferers increases excessively, the probability of having more than two interferers creating a destructive IM3 component increases.

Finally, it is worth mentioning that the proposed solution in this paper suits the lower end of the CR band, as this part is more susceptible to harmonic mixing. For instance, assume a communication channel that is located above 400 MHz. In this case, even by employing direct conversion receivers, the LO harmonics fall outside the receiving band, particularly if the receiver incorporates 3^{rd}, and 5^{th} harmonic rejection architecture. Therefore an optimal solution can be to break down the CR band into two parts, and to employ a heterodyne architecture (as described in this paper) for the lower band, and a harmonic rejection direct conversion receiver for the upper band. This can help the heterodyne receiver part in two major ways by lowering the total bandwidth it should cover; first, the active feedback loop, and second, the LO generation. The LNA can be designed with active load without gain-bandwidth trade-off, therefore improving the NF of the receiver. The active feedback loop can also filter wider bandwidth interferers, and employing passive mixer in the feedback path becomes less challenging, which can enhance NF as well. And finally, the intermediate frequency of the heterodyne conversion (first step) does not need to be pushed to very high frequencies in order to achieve higher harmonic rejection, since the LNA gain in this case would roll off at lower frequencies, providing more attenuation at a given frequency outside the receiving band.

[14]The probability oh this situation to take place is $\frac{1}{\mathrm{N_{Ch}}}$, where $\mathrm{N_{Ch}}$ is the number of available channels.

2.8 Summary

An ultra-wideband receiver based on heterodyne up-down conversion scheme is presented for CR applications to mitigate the LO harmonics mixing problem and enable the receiver to work in VHF frequency range. It was shown that by employing this architecture, the potential interferers that can coincide with the signal through harmonic mixing process are pushed to frequencies well beyond the receiving band and therefore attenuated by as much as 70 dB, regardless of the harmonic number. Also by means of employing an active feedback loop, the receiver can reject and therefore tolerate strong interferers to protect the desired signal from the potential intermodulation destruction. The heterodyne-conversion part exploits current-driven passive mixer architecture and is optimized to provide high linearity. Analytical calculation as well as system-level simulations and measurements have been presented to model and characterize the linearity and NF performance of the receiver.

3. ULTRA-LOW POWER RECEIVER

3.1 Super-Regenerative Oscillator and the Need for an Ultra-Low Power Receiver

The rapid growth of the wireless communication market has persisted over the past years, and by the advent of the Internet-of-Things (IoT) notion, and desire for a ubiquitous wireless connection, the demand for more flexible and versatile wireless devices and communication is ever-increasing. There still remains a number of major challenges to be addressed on the way to fully realizing IoT world, one of which is power consumption. To maintain a reliable wireless link between an access point, and, for an example, a smart toy, over a comparatively long distance and long period of time, the smart toy should be empowered with an Ultra-Low Power (ULP) transceiver that at the same time offers reasonable performance. Medical Implant Communication Service (MICS), Wireless Sensor Networks (WSN), and Wake-Up Radio (WUR) applications are also examples of areas that having an ULP transceiver seems appealing.

Various architectures for ULP receivers have been recently studied, and plenty of works have offered decent performance while lowering the power consumption to mW and sub-mW range [55–78]. Among all the differences and similarities of these works, they can be differentiated on the basis of their architecture into two generic categories: 1) linear receivers [55–62]; in which a local oscillator (LO) signal is used to down-convert the desired signal from radio frequencies to baseband, and 2) nonlinear, envelope detector based receivers [63–78]. The latter category is more suitable for simple modulation schemes, in which demodulation is performed by extracting the data overlaid in the envelope of the incoming signal, using an envelope detector. Fig. 3.1 depicts simple block diagrams of such ULP receivers. Linear receivers (Fig. 3.1(a)) tend to be more robust, however more power consuming. Channel selection is done by the synthesizer and gain

and NF of the receiver is less sensitive to PVT variations. On the other hand, a synthesizer consumes significant portion of the power budget, limiting linear receivers to mW range. Although sub-mW linear receivers have been reported through innovative low-power circuit design techniques, they usually compromise the performance of the Local Oscillator (LO) generation block, which is the most important advantage of linear architecture over the other group. For instance, [55] employs a ring oscillator for LO generation, resulting in poor phase noise, and consequently sensitivity. Similarly, [59] relies on injection locking to an external LO signal, to improve the phase noise of its internal VCO, and [62] completely assumes external LO signals. In another example, [61] uses an extremely low-voltage supply, and in that way requires as many as eleven on-chip inductors to realize an accommodating circuitry.

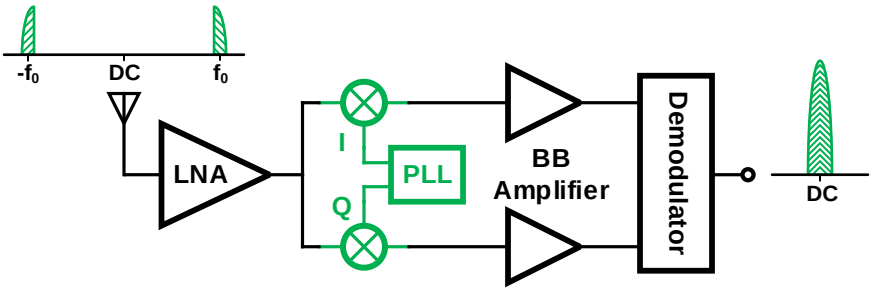
Nonlinear receivers, on the other hand, are inherently low power, however more prone to interference, and less robust. Nonetheless, they can be differentiated in three sub-categories:

1. Uncertain-IF receivers (UIF) [63–67], where a free running ring oscillator realizes the LO signal that down-converts the desired signal to an uncertain IF, from which point the data is extracted by means of an envelope detector (Fig. 3.1(b)).

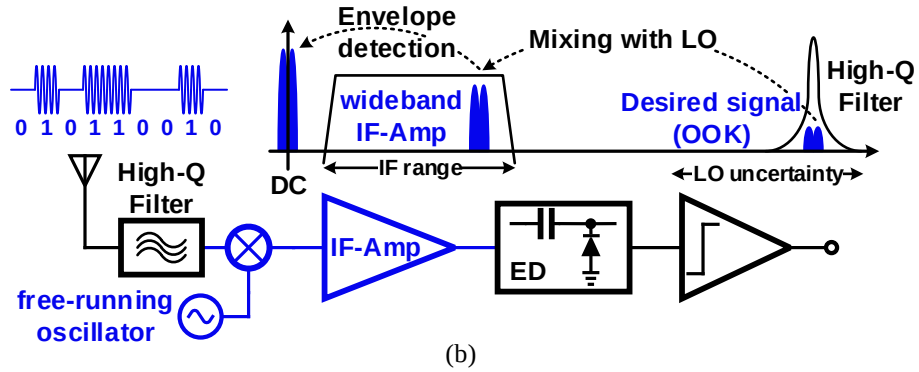
2. Super-Regenerative receivers (SRR) [68–76], which is based on super-regenerative oscillator (SRO) architecture and there is no explicit frequency conversion scheme (Fig. 3.1(c)).

3. Injection Locking Oscillator (ILO) receivers [77, 78], which is similar to SRO, and uses a tuned oscillator as a frequency to amplitude conversion block to extract FSK-modulated data from the incoming signal (Fig. 3.1(d)).

UIF receivers are susceptible to interference, since they indiscriminatingly down-convert a wide range of frequency spectrum to the baseband through an envelope detection, and



(a)



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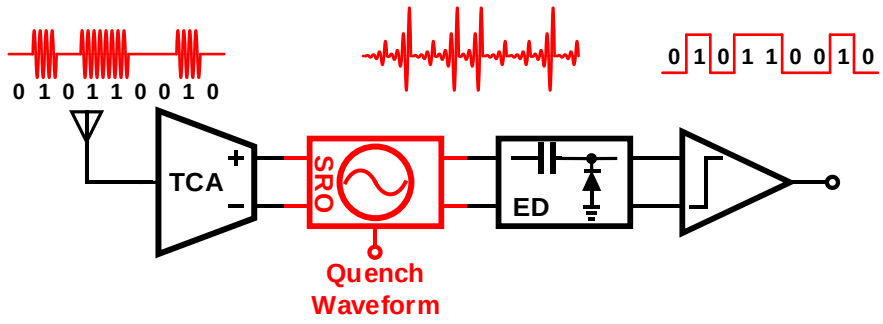

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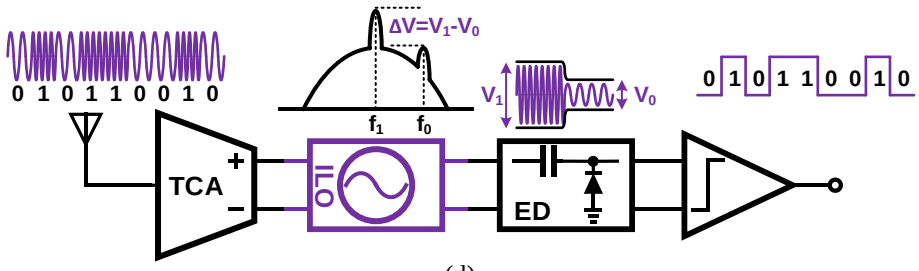


(d)

Figure 3.1: Conceptual block diagram and functionality of (a) Linear, (b) Uncertain-IF, (c) Super-Regenerative, and (d) Injection-Locking receivers.

therefore usually require a high-Q input filter. ILO receivers' architecture is similar to that of SRR, although the reception mechanism is different. An ILO employs a tuned oscillator and injection locking concept [79] to receive and demodulate an FSK-modulated signal, while an SRR modulates the bias current of its oscillator and relies on the transient response of the oscillator. As such, an SRR is capable of receiving OOK, and ASK, in addition to FSK modulation. Moreover, modulating the bias current of the oscillator, as will be discussed in Section 3.2, can theoretically result in a more selective bandpass filter, compared to an oscillator with a constant bias current as in ILO receivers. Therefore it is possible for an SRR to achieve better performance than that of an ILO counterpart, in similar conditions. Fig. 3.2 plots energy efficiency versus sensitivity along with FoM contours for recent sub-mW ULP receivers.

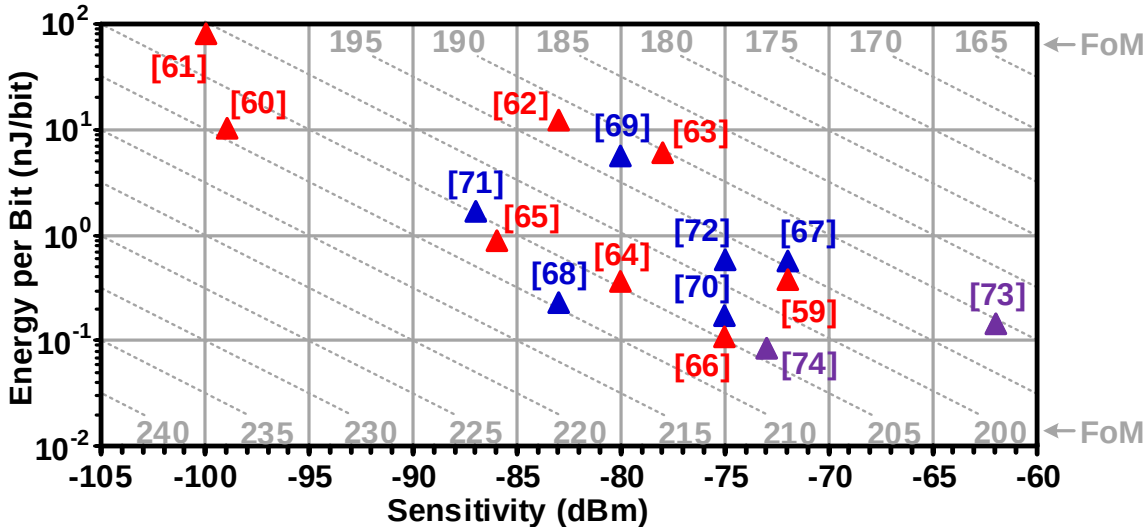


Figure 3.2: State-of-the-art ultra-low power wake-up receivers: SRR (red data points), UIF (blue data points), and ILO (violet data points).

While SRR can provide decent performance even at sub-100 μW range it suffers from some fundamental challenges that this paper tries to address. For instance, an SRR re-

quires multiple calibration schemes to guarantee its proper performance. Without the required calibrations, the SRR performance could degrade significantly. Chen, et. al [75], has offered such calibration measures, however, this has dramatically increased power consumption; it employs a fractional-N synthesizer that needs to be running incessantly, except for short period of reception, to set the operating frequency. As will be explained in Section 3.3, the amplitude variation of the SRO can also cause an unknown frequency offset between the desired channel and its operating frequency. The presented work in this paper utilizes an amplitude lock loop (ALL) to set the amplitude of the oscillation at a constant level to address this issue.

There is also a trade-off between sensitivity and power consumption on one hand and the power of the back-radiated signal on the other hand. For instance [72–74] have removed the input isolating amplifier from the receiving path, and by doing so improved sensitivity and significantly lowered the power consumption. However the back-radiated signal in these cases could potentially be strong and depending on different regulations might not be allowed. This trade-off is studied in Section 3.2 in more depth. Integrability is another challenge; in order to improve the receiver performance, particularly power consumption, sensitivity and selectivity, many works [71–74] have incorporated external components. Bohorquez et. al [74] is employing a custom designed antenna as the resonator, and [71] needs as many as six external components in addition to a balun, making them less attractive for low-cost applications. Rezaei, et. al [80] has reported a fully-integrated receiver that incorporate various calibration schemes to ensure the proper functionality of the receiver while achieving the best performance of a fully-integrated SRR. In this paper the authors show that the proposed receiver is quite flexible in terms of trading off data rate for sensitivity. In contrast to conventional OOK receivers, here an ADC is employed to convert the received signal, and by doing so has enabled the PHY layer to spread a low data rate signal on a higher baud rate stream and gain a remarkable sensitivity improvement.

The rest of this chapter is organized as follows. Section 3.2 reviews the generic theory behind a SRR trying to provide insights into the complex mathematical studies published regarding the super-regenerative systems. Section 3.3 presents the proposed receiver architecture and examines the practical issues inherited in this concept, and measures to mitigate these problems. The circuit implementation is explained in Section 3.4 and provides the simulation results of the key building blocks. Extensive measurements data are presented in Section 2.6, and finally Section 3.6 concludes this chapter.

3.2 General Theory of Super-Regeneration

An SRR, as seen in Fig. 3.3(a), constitutes an input transconductance amplifier (TCA) isolating the antenna from, and coupling the incoming signal to the SRO, an Envelope Detector (ED) extracting the amplitude of the oscillation, and a comparator that decides whether or not the received signal was *Zero* or *One*, based on the amplitude of oscillation. The SRO can be modeled as a parallel resonant circuit as shown in Fig. 3.3(b), however, unlike conventional oscillators with constant negative conductance and steady oscillation, the negative conductance in a SRO is modulated, with a periodic signal usually called the *quench* signal, and therefore the oscillation repeatedly grows and decays. The presence or absence of the incoming signal affects the transient response of the oscillator and its oscillation build-up. As seen from Fig. 3.3(c), when the SRO is coupled with a tuned input signal, the oscillation starts faster and therefore grows larger than the case where there is no input signal and the oscillation builds up merely due to noise. due to noise.

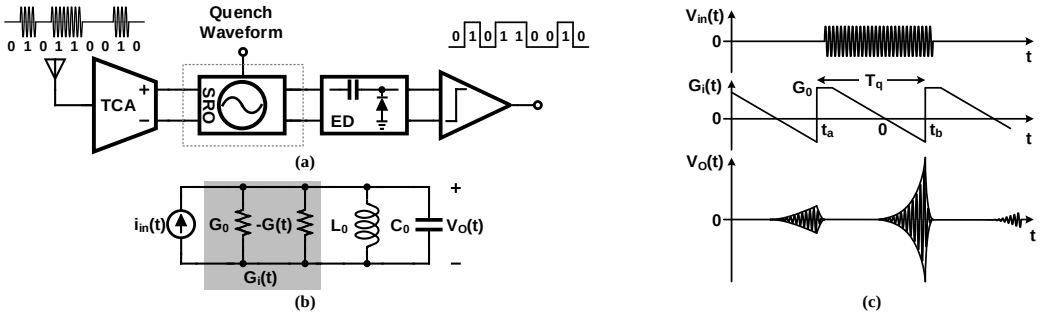


Figure 3.3: (a) Simple block diagram of the SRR. (b) The parallel resonant RLC model of a SRO. (c) Generic example of a SRO oscillation amplitude with and without injected signal.

SR idea dates back to early days of electronics design [81] and has been rigorously studied ever since [82–87]. For the most part, these studies are similar in approach and

results, and start from the characteristic differential equation of system Fig. 3.3(b) as following [86]

$$\frac{d^2V_O\left(t\right)}{dt^2}+\frac{G_i\left(t\right)}{C_0}\frac{dV_O\left(t\right)}{dt}+\left({\omega_0}^2+\frac{1}{C_0}\frac{dG_i\left(t\right)}{dt}\right)V_O\left(t\right)=\frac{1}{C_0}\frac{di_{in}\left(t\right)}{dt} \tag{3.1}$$

in which $\mathrm{G_i\left(t\right)=G_0-G\left(t\right)}$ is the instantaneous conductance of the tank, and $\omega_0=\frac{1}{\sqrt{\mathrm{L_0C_0}}}$ is the center frequency of the resonant network. It is clear from (3.1) that the behavior of SRO is strongly affected by how $\mathrm{G_i\left(t\right)}$ varies, during the excursion of $\mathrm{G\left(t\right)}$. Based on this fact, we can divide the quench cycle into two general sections; 1) when $\mathrm{G_i\left(t\right)>0}$ during which the free oscillation extinguishes as the active devices cannot provide enough energy to compensate for the intrinsic loss of the tank, and 2) when $\mathrm{G_i\left(t\right)<0}$ in which the oscillation builds up from the excitation $\mathrm{i_{in}\left(t\right)}$, and as long as $\mathrm{G_i\left(t\right)<0}$ the oscillation grows exponentially[1]. As shown in [86], the particular solution, $\mathrm{V_{O_p}}$, for the differential equation (3.1), when $\mathrm{i_{in}\left(t\right)=I_0\cos\left(\omega_i t\right)}$ can be expressed as

$$V_{Op}\left(t\right)=K_sp\left(t\right)\frac{I_0\omega_i}{C_0\omega_0}\int_t^{t_a}s\left(\tau\right)\sin\left(\omega_i\tau\right)\sin\left(\omega_0\left(t-\tau\right)\right)d\tau \tag{3.2}$$

where $\mathrm{K_s}$, $\mathrm{p\left(t\right)}$, and $\mathrm{s\left(t\right)}$ are super-regenerative gain, normalized output envelope, and the sensitivity curve of the SRO, and are defined as

$$K_s=\ exp\left(\frac{-1}{2C_0}\int_0^{t_b}G_i\left(\tau\right)d\tau\right) \tag{3.3a}$$

$$p\left(t\right)=\ exp\left(\frac{1}{2C_0}\int_t^{t_b}G_i\left(\tau\right)d\tau\right) \tag{3.3b}$$

$$s\left(t\right)=\ exp\left(\frac{1}{2C_0}\int_0^{t}G_i\left(\tau\right)d\tau\right). \tag{3.3c}$$

By defining $\mathrm{S\left(\omega\right)=\mathcal{F}\{s\left(t\right)\}}$ as the Fourier transformation of the sensitivity curve $\mathrm{s\left(t\right)}$,

[1] At least at the outset of the oscillation when the oscillation amplitude has not become current starved and saturated.

(3.2) can be estimated by

$$V_{Op}(t) \approx K_s K_r p(t) \frac{I_0}{G_0} |H_{BPF}(\omega_i)| \cos(\omega_0 t + \angle S(\omega_0 - \omega_i)) \tag{3.4}$$

where $\mathrm{K_r} = \frac{\mathrm{G_0}}{2\mathrm{C_0}}\mathrm{S}(0)$ is the SRO regenerative gain, and $\mathrm{H_{BPF}}(\omega)$ models a bandpass filter around ω_0 that governs the frequency response of the SRR to the input excitation signal $\mathrm{i_{in}}(\mathrm{t})$, defined as

$$H_{BPF}(\omega) = \frac{\omega S(\omega_0 - \omega)}{\omega_0 S(0)}. \tag{3.5}$$

Equation (3.4) suggests that the SRO output voltage fundamentally depends on the behavior of $\mathrm{G_i}(\mathrm{t})$, therefore it is essential to establish a method that can predict the performance of a SRR, given the parameters of such system[2] and its corresponding $\mathrm{G_i}(\mathrm{t})$ signal. Assuming a simple OOK modulation, to find the BER of a given SRR at a given input signal power level, the probability density function (PDF) of the peak SRO output voltage should be found in two cases; first, when there is no excitation at the input and oscillation starts due to the system noise (which is interpreted as *Zero*), and second, when the incoming signal at ω_0 with power $\mathrm{P_{in}}$ is applied to the input (and is interpreted as *One*). Consider Fig. 3.4 in which $\overline{\mathrm{v^2_{n,in}}}$ models the input referred noise of the SRR, including noise of the antenna and receiver, that is noise due to $\mathrm{G_{m,TCA}}$ block, tank loss $\mathrm{G_0}$, and negative conductance block $-\mathrm{G}(\mathrm{t})$. Therefore the injected noise current into the SRO tank, ie $\overline{\mathrm{i^2_{n,inj}}}$, can be related to the receiver NF as following

$$\overline{i^2_{n,inj}} = \overline{(i_{n,inj+} - i_{n,inj-})^2} = G^2_{m,TCA}\overline{v^2_{n,in}} = 4kTR_S G^2_{m,TCA} NF. \tag{3.6}$$

Note that the NF in (3.6), that is also being used in the analysis presented in this section, refers to the small signal model for a linear RLC network as shown in Fig. 3.4.

[2]Such as noise figure, the resonator components value and quality factor, the input amplifier transconductance, and etc.

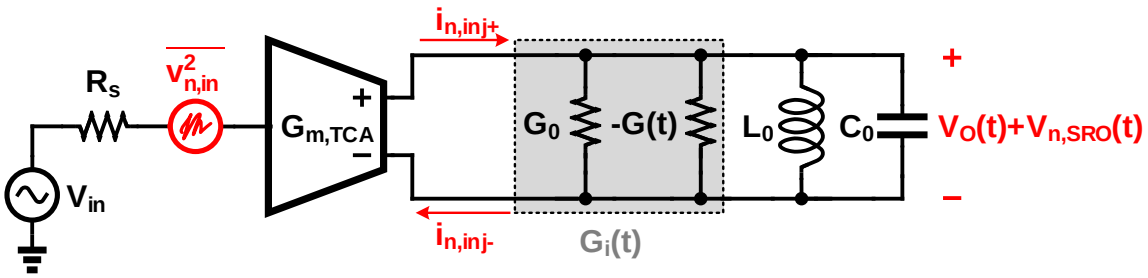


Figure 3.4: Simple noise model of a generic SRO and input isolating amplifier.

The NF calculated in this way depends weakly on the variation of $-\mathrm{G}\left(\mathrm{t}\right)$, therefor it can be calculated around $-\mathrm{G_i}\left(\mathrm{t}\right) \approx 0$, and assumed constant elsewhere.

When there is no signal at the input of the SR receiver (the case of input *Zero*), the SRO output voltage $\mathrm{V_O}$ is merely generated due to the injection of $\overline{\mathrm{i^2_{n,inj}}}$ into the SRO tank. Assuming $\overline{\mathrm{i^2_{n,inj}}}$ has a white noise profile, the resulting noise voltage can be modeled as a bandpass noise [88], where the SRO tank frequency response is represented by (3.5), therefore the bandpass noise can be expressed in quadrature form as

$$V_{n,SRO}\left(t\right) = V_{n,SRO,i}\left(t\right)\cos\left(\omega_0 t\right) - V_{n,SRO,q}\left(t\right)\sin\left(\omega_0 t\right) \tag{3.7}$$

with $\overline{\mathrm{V^2_{n,SRO,i}}} = \overline{\mathrm{V^2_{n,SRO,q}}}$ as the in-phase and quadrature components. Substituting (3.6) into (3.4), to find the power of the in-phase and quadrature noise component results in

$$\overline{V^2_{n,SRO}} = \overline{V^2_{n,SRO,i}} = \overline{V^2_{n,SRO,q}} = \underbrace{K_r^2 K_s^2 \frac{G^2_{m,TCA}}{G_0^2}}_{A^2_{SR}} \underbrace{4kTR_S NF}_{\overline{v^2_{n,in}}} \Delta f_{ENB} = A^2_{SR}\overline{v^2_{n,in}}\Delta f_{ENB} \tag{3.8}$$

where $\mathrm{A_{SR}}$ is the SR receiver small signal gain, and $\Delta\mathrm{f_{ENB}} = \int_0^\infty \left|\mathrm{H_{BPF}}\left(\mathrm{f}\right)\right|^2 \mathrm{df} = \alpha \mathrm{f_q}$ is the equivalent noise bandwidth (ENB) of the SRO tank frequency response. Note that α is a coefficient that is determined by the shape of the quench signal and $\mathrm{f_q}$ is the quench

signal frequency. The envelope of the SRO output voltage due to input *Zero*, $\mathrm{V_{O,Zero}}$ can be then found as

$$V_{O,Zero} = \sqrt{V_{n,SRO,i}^2 + V_{n,SRO,q}^2}. \tag{3.9}$$

The peak voltage of the SRO output voltage envelope in this case, has a Rayleigh distribution [88], and its PDF can be expressed as

$$PDF_{Zero}\left(V\right) = \frac{V}{\overline{V_{n,SRO}^2}} e^{-\frac{V^2}{2\overline{V_{n,SRO}^2}}} U(V) \tag{3.10}$$

where $\mathrm{U(V)}$ is the unit step function.

In the case of input *One*, the incoming signal $\mathrm{V_{in}}$ is amplified by the small signal gain of the SR receiver ($\mathrm{A_{SR}}$) and is added to the bandpass noise of the SRO tank in (3.7), and therefore the SRO output voltage becomes

$$V_{O,SRO}\left(t\right) = A_{SR}V_{in}\cos\left(\omega_0 t\right) + V_{n,SRO,i}\left(t\right)\cos\left(\omega_0 t\right) - V_{n,SRO,q}\left(t\right)\sin\left(\omega_0 t\right) \tag{3.11}$$

and the envelope of the SRO output voltage due to input *One*, $\mathrm{V_{O,One}}$ can be found as

$$V_{O,One} = \sqrt{\left(A_{SR}V_{in} + V_{n,SRO,i}\right)^2 + V_{n,SRO,q}^2}. \tag{3.12}$$

The envelope of $\mathrm{V_{O,One}}$ has a Rician distribution [89] with a PDF expressed as

$$PDF_{One}\left(V\right) = \frac{V}{\overline{V_{n,SRO}^2}} e^{-\frac{V^2 + A_{SR}^2 V_{in}^2}{2\overline{V_{n,SRO}^2}}} I_0\left(\frac{A_{SR}V_{in}V}{\overline{V_{n,SRO}^2}}\right) U(V) \tag{3.13}$$

where $\mathrm{I_0\left(V\right) = \frac{1}{\pi}\int_0^{\pi} e^{V\cos\phi} d\phi}$ is the modified Bessel function of the first kind and order zero.

In contrast to [89], here we determine the BER of the receiver at the output of the

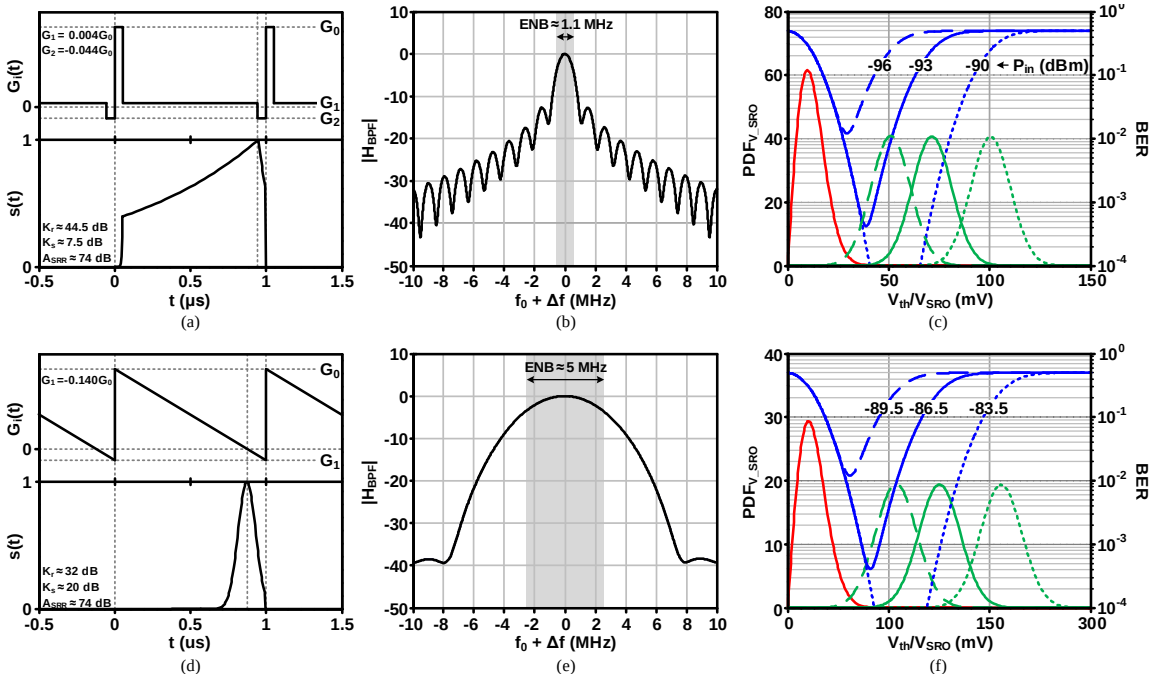


Figure 3.5: Two simple cases of $\mathrm{G_i\,(t)}$; Left column shows the $\mathrm{G_i\,(t)}$ signals and the corresponding sensitivity curves $\mathrm{s\,(t)}$. The frequency response of the SRO tank regarding the presented $\mathrm{G_i\,(t)}$ signal and its ENB is depicted in the middle. The right column shows the PDF of the SRO output amplitude for *Zero* (red curves), and *One* (green curves) input with three different power levels, versus the SRO amplitude $\mathrm{V_{SRO}}$, and the corresponding BER curves (blue curves) versus the threshold voltage $\mathrm{V_{th}}$.

SRO instead of the ED[3], for three reasons; first, the small signal gain of the SR receiver is comparatively high enough[4] to neglect the additive noise of the following stages, second, the ED can have a nonlinear gain profile[5] complicating the calculation of final PDFs, and third, excluding the ED, makes it possible to provide a more intuitive insight into the performance of SR receiver and the corresponding contributing factors. Therefore assuming a pseudo-random sequence with equal *Zero*s and *One*s probability for the incoming OOK signal, the BER of the SR receiver can be calculated from

$$BER = \frac{1}{2}\int_{V_{th}}^{\infty} PDF_{Zero}\left(V\right) dV + \frac{1}{2}\int_{0}^{V_{th}} PDF_{One}\left(V\right) dV \tag{3.14}$$

where $\mathrm{V_{th}}$ is the comparator threshold voltage; the incoming data is interpreted as *One*, if the peak voltage is higher than $\mathrm{V_{th}}$, and *Zero* if it is lower.

Although (3.14) provides an accurate measure to find the SR receiver BER, at a given input signal level, it is not an intuitive measure. It is more intuitive to find the sensitivity of the SR receiver, $\mathrm{P_{sen}}$, at a given BER. To do so, the SNR at the output of the SRO, $\mathrm{SNR_{SRO,out}}$, can be found and equated to the minimum SNR that is required to detect the incoming OOK signal at a certain BER, $\mathrm{SNR_{SR,min}}$, as following

$$SNR_{SR,min} = SNR_{SRO,out} = \frac{\mu_1\left(PDF_{One}\right)^2}{\mu_1\left(PDF_{Zero}\right)^2} \approx \frac{A_{SRR}^2 V_{in}^2}{\frac{\pi}{2}\overline{V_{n,SRO}^2}} \tag{3.15}$$

where $\mu_1\left(\mathrm{PDF_X}\right)$ is the expected value of random variable X. It is important to note that random variables represented by $\mathrm{PDF_{One}}$, and $\mathrm{PDF_{Zero}}$, are the oscillation amplitude of the SRO, for the input signals *One*, and *Zero*, respectively. Therefore $\mu_1\left(\mathrm{PDF_{One}}\right)^2$, and $\mu_1\left(\mathrm{PDF_{One}}\right)^2$ correspond to the signal and noise power at the output of the SRO.

[3]The ultimate BER should be measured/calculated at the output of the final comparator.
[4]Normally more than 50 dB.
[5]Which for instance is the case in this design, and will be discussed in Section 3.4

Equation (3.8) can be substituted into (3.15), and then rearranged to find the sensitivity of the receiver as

$$P_{sen} = -174 + NF + SNR_{SR,min} + 10\log\left(\frac{\pi}{2}\Delta f_{ENB}\right). \tag{3.16}$$

Equation (3.16) is similar to the sensitivity of conventional linear receiver, except for the bandwidth. In conventional linear receivers, demodulation is being carried out at the base-band, where a sharp filter can select the desired signal band and filter out the rest. In this case, the noise bandwidth that is used to calculate sensitivity is limited to the signal bandwidth. This is not the case in a SR receiver; the noise bandwidth in (3.16) is determined by the selectivity of the SR oscillator, or in other word the ENB of the bandpass filter $\mathrm{H_{BPF}}$ in (3.5). Fig. 3.5 illustrates the performance of a generic SRR in two simple $\mathrm{G_i\,(t)}$ cases, with such attributes that result is similar $\mathrm{A_{SRR}}$ for better comparison. As seen from Fig. 3.5(a), in a pulse shaped quench signal, $\mathrm{G_i\,(t)}$ is just above zero for most of the cycle, and abruptly jumps to a negative value, resulting in a wide sensitivity function $\mathrm{s\,(t)}$, and narrow $\mathrm{H_{BPF}\,(\omega)}$ (Fig. 3.5(b)). Using (3.10)-(3.14), $\mathrm{PDF_{Zero}}$, $\mathrm{PDF_{One}}$, and the BER curves of the system for different input signal power can be estimated. Fig. 3.5(c) depicts two graphs mapped into a single plot; 1) $\mathrm{PDF_{Zero}}$, $\mathrm{PDF_{One}}$ at different $\mathrm{P_{in}}$ levels versus SRO output voltage ($\mathrm{V_{SRO}}$), and 2) the corresponding BER curves versus a hard-decision decoder threshold voltage $\mathrm{V_{th}}$. For instance, for a -93 dBm input, the BER reaches as low as $4{\times}10^{-4}$ when $\mathrm{V_{th}} \approx 40\ \mathrm{mV}$. Fig. 3.5(d), in contrast, shows a simple sawtooth quench signal in which $\mathrm{G_i\,(t)}$ starts from $\mathrm{G_0}$ and linearly increases during the quench cycle. This results in a much narrower $\mathrm{s\,(t)}$, and wider $\mathrm{H_{BPF}\,(\omega)}$ with higher ENB. Recalling from (3.16), at a certain BER level, the sensitivity of the sawtooth quench signal suffers from its excess ENB. Considering Fig. 3.5(b) and (e), $\frac{\mathrm{ENB_{sawtooth}}}{\mathrm{ENB_{pulse}}} = \frac{5}{1.1} \approx 6.5\ \mathrm{dB}$, which is translated to the sensitivity difference for identical BER level in Fig. 3.5(c) and (f).

3.3 Receiver Architecture

Fig. 3.6 shows a simple block diagram of the designed SR receiver including its calibration loops. The receiver works in three modes; 1) Frequency calibration mode, in which the center frequency of the SRO tank is tuned to the desired signal frequency, 2) Critical current detection mode, where the SRO critical bias current is being searched for and found, and 3) RX-mode, in which the SR receiver is working and demodulating the incoming OOK signal.

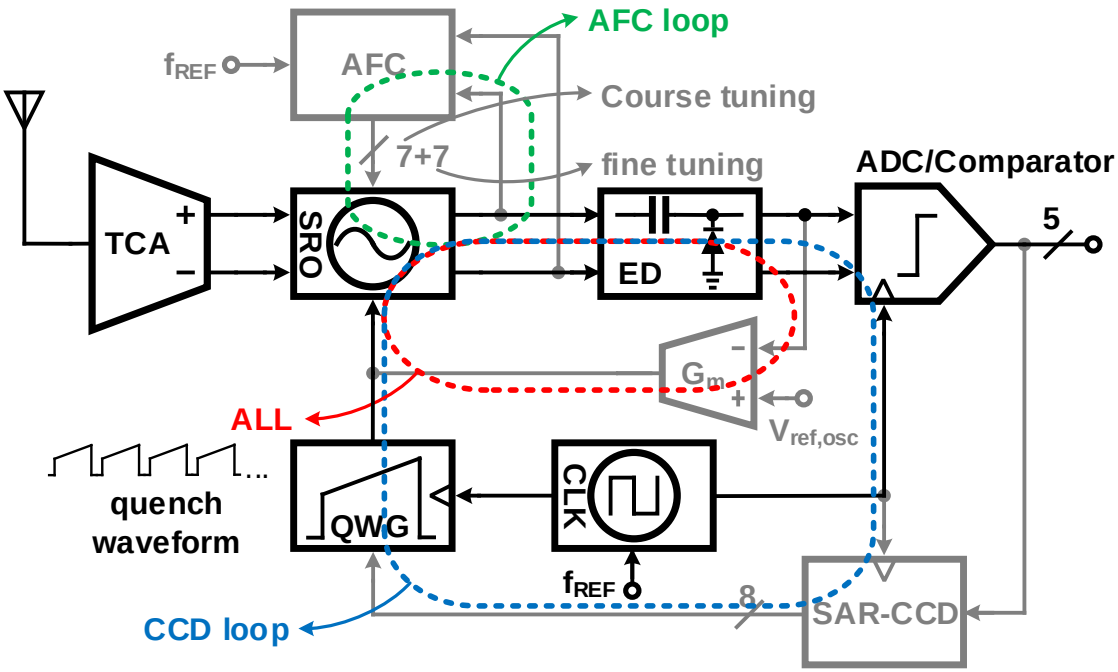


Figure 3.6: The block diagram of the designed SRR, including calibration loops.

3.3.1 Calibration Modes

In conventional linear receivers, the down-conversion of the desired signal is done by means of multiplying it with a Local Oscillator (LO) signal. Although it is a power hungry block, a synthesizer can precisely control the reception frequency of the receiver. In an SR receiver however, the center frequency of the SRO tank circuit determines the reception frequency of the receiver, therefore a frequency calibration scheme is necessary to ensure its proper performance. Chen, et al. [75], has employed a VCO (as the SRO) and a programmable integer-N PLL to adjust the resonance frequency of the SRO tank. When the calibration phase is over, the varactor voltage is held on a capacitor, the PLL is powered down and the receiver transits to RX-mode. The voltage captured by the capacitor is subject to, mainly, leakage and coupling with other signals and needs to be updated rather frequently, which drastically increases the power consumption. In this design, a DCO is employed at the core of the receiver as the SRO. This enables to digitally control the frequency of the SRO and rid the need for frequent calibration cycles, reducing the power consumption. In this case, the frequency calibration is only needed, when the operating frequency changes. Regardless of the method used to adjust the desired frequency, there is always an intrinsic error associated with the calibration scheme.

Regardless of method used to adjust the desired frequency, there is an intrinsic error associated with the calibration scheme. Consider Fig. 3.7 in which a conventional NMOS cross-coupled LC oscillator is depicted. To measure and therefore adjust the operating frequency, the oscillator needs to oscillate with some non-zero oscillation amplitude. The oscillation frequency can be found from

$$f_{SRO} = \frac{1}{2\pi\sqrt{L_0\left(C_0 + \frac{C_{Par}}{2}\right)}} \tag{3.17}$$

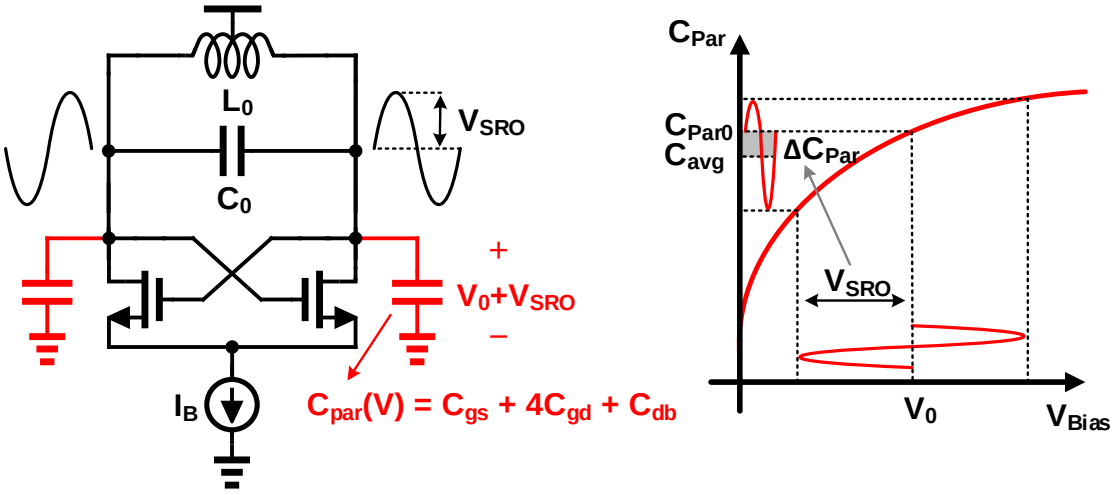


Figure 3.7: (a) The effect of non-linear parasitics on the frequency calibration. (b) Different oscillation amplitude, results in different parasitics value, and an offset frequency Δf.

where $C_{Par} = C_{gs} + 4C_{gd} + C_{db}$ is the nonlinear voltage-dependent parasitics of the cross-coupled NMOS transistors. As seen from Fig. 3.7(b), at zero oscillation amplitude (i.e., $V_{SRO} = 0$), the parasitics caps are biased at V_0. At non-zero oscillation amplitude, this bias point becomes modulated, and as a result of a nonlinear characteristics, the average parasitics capacitance that the tank circuitry senses decreases. It is impossible to set the exact operating frequency at the operating bias point of the SRO, since the SRO (in contrast with a conventional oscillator) for the most part works in the quenched mode, where there is little or no oscillation. This means there would be an inevitable offset between the desired operating frequency and the calibrated one. The larger the amplitude of the oscillation is, the more deviation is introduced into C_{Par} and consequently f_{SRO}. This offset remains constant as long as the amplitude of the oscillation kept unchanged, otherwise the offset varies unpredictably with the unknown amplitude of the oscillation. One way to keep the amplitude of the oscillation constant is to inject enough bias current into the

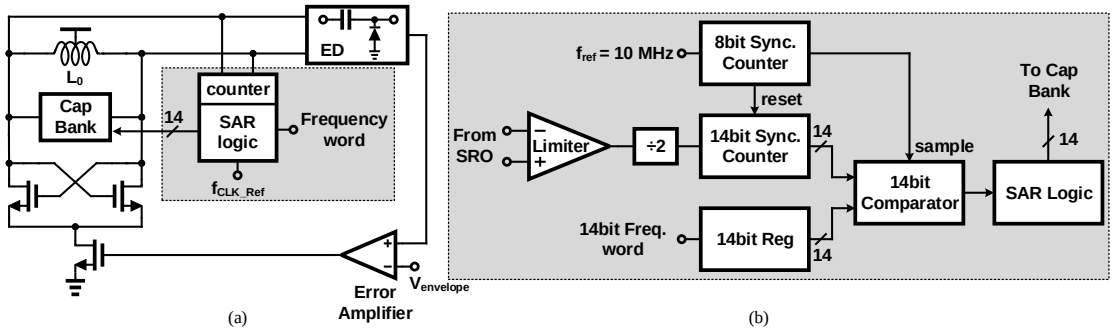


Figure 3.8: (a) Amplitude lock loop (ALL) keeps the oscillation amplitude at a constant and low level. (b) Automatic frequency calibration (AFC) sets the working frequency through a binary search algorithm done by 14-bit SAR.

SRO to make the oscillation amplitude voltage limited. Although this makes the offset frequency constant and predictable, it results in the largest offset and requires comparatively large[6] bias current. An alternative approach, as shown in Fig. 3.8 is to employ an Amplitude Lock Loop (ALL), that works simultaneously with the Automatic Frequency Calibration (AFC) block, keeping the amplitude of the oscillation at a constant and low level. Not only this approach saves power during calibration phases, but also mitigates the leaked back-radiated oscillation as much as about 20 dB.

The AFC which is comprised of two 14-bit and 8-bit synchronous counters and a successive approximation register (SAR) unit, performs a binary search to set the SRO operating frequency. As shown in Fig. 3.8(b), the 8-bit counter, shares the same reference 10 MHz clock used to control Quench signal. It periodically counts from zero to a programmable number $\mathrm{N_{count8}}$, resulting constant cycles of $\mathrm{T_{count}} = \frac{\mathrm{N_{count8}}}{10}$ μs. During these cycles, the 14-bit counter counts the zero crossings of a buffered, and divided by 2 version of the SRO output. At the end of each cycle, the result of this countdown is compared to a preset frequency control word, to determine whether or not the SRO frequency is below or above the target frequency. This approach, although simple, results in two major issues;

[6]Typically ten times as much the SRO consumes in the RX mode

first, there is a frequency error of $|\Delta f_{DCO}| \leq \frac{1}{T_{count}}$ in the final result, and, second, the power consumption of the 14-bit counter is significantly high, as it is clocked at the SRO frequency. However, since the receiver does not require frequent frequency calibration, N_{count8} can be increased to reduce the frequency calibration error, with negligible overall power penalty. The AFC which is comprised of a counter and a successive approximation register (SAR), performs a binary search to set the SRO operating frequency. It counts the zero crossings of the SRO oscillation in a given fixed period, computes the average frequency, and based on the provided frequency word, determines the SRO state of the capacitor bank within 14 steps.

A similar approach is employed to detect the critical current of the SRO. Once the frequency calibration is complete, and the capacitor bank state is stored accordingly, another binary search loop, as shown in Fig. 3.9, is activated to detect the critical bias current of the SRO. This method also intrinsically bears the offset problem.

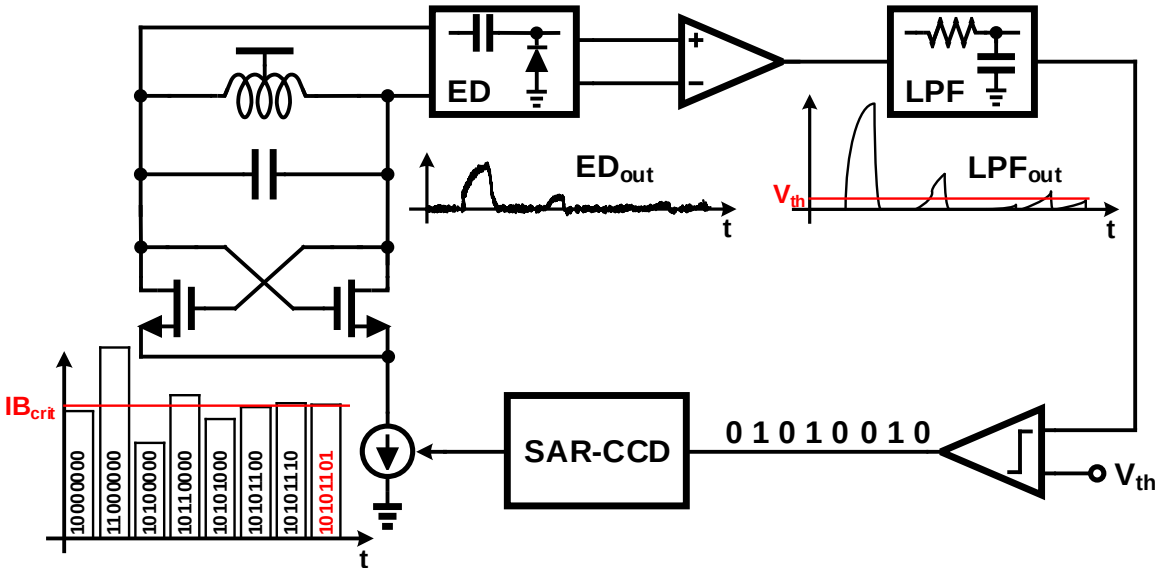


Figure 3.9: Critical current detection (CCD) loop. Simulations showed this architecture can find IB_{Crit} with around %1 accuracy, therefore an 8-bit SAR is employed to acquire this resolution.

Theoretically, the critical current ($\mathrm{IB_{crit}}$) is defined as the point at which $\mathrm{G_i\,(t)} = 0$, or in other word the oscillation is about to start, and therefore it is impossible to detect the exact critical current. Simulation shows $\mathrm{IB_{crit}}$ can be found with around $\%1$ accuracy, therefore an 8-bit SAR is employed to realize the binary search. Once $\mathrm{IB_{crit}}$ is detected, the quench wave generator (QWG) module, generates the quench signal proportionally, which is described in Section 3.4.4.

3.3.2 RX Mode; Soft Decisioning and Data Rate-Sensitivity Trade-off

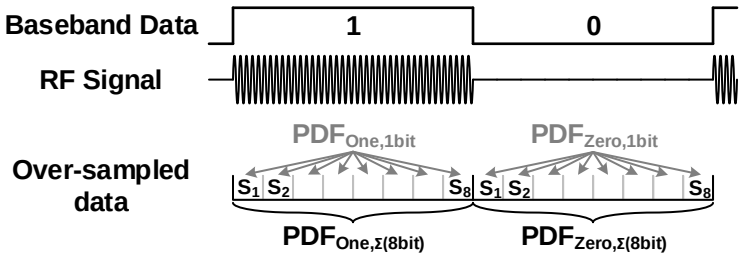
In this mode, calibration loops are all off, and the clock generator module synchronizes the ADC and quench signal. The envelope of the SRO reaches its peak exactly at the end of the quench signal cycle, and is quenched steeply at the beginning of the next cycle, therefore the output of ED is sampled exactly at the end of the cycle. Since the SRR is non-coherent, the sampling rate should be at least twice the data baud rate to adhere to the Nyquist criteria. The SRR is a sample data system, where it samples the envelope of the RF signal every quench period. Recalling (3.16), doubling the sampling rate, or in other word quench frequency $\mathrm{f_q}$, doubles the ENB of the SRO tank frequency response ($\mathrm{H_{BPF}}$) and consequently degrades the sensitivity by 3 dB[7]. This design, employs an ADC, enabling soft-decision decoding of the received data stream. In the conventional way of using a comparator and hard-decision decoding, the sensitivity suffers from the higher quench rate. For instance, when $\mathrm{f_q} = 2\mathrm{f_{Baud}}$, the second sample bears no additional info; it is either the same as the first one (00 or 11), in which case it is interpreted as the incoming data (0 or 1), or it is contradictory (01 or 10), where the output is not valid. However, by employing an ADC and soft-decision decoding, the amplitude of the ED output, as a measure of the signal power, can be extracted and the decision can be made from the accumulation of the consecutive samples amplitude. In fact, the soft-decision decoding can improve sensitivity by about 2.2 dB [90]. Moreover, this technique can be extended by means of oversampling the incoming data to improve the sensitivity even more. Fig. 3.10(a) shows conceptual baseband, RF, and oversampled signals for an 8X oversampling receiver. Higher data rate can be traded off to employ higher oversampling rate and therefore achieving better sensitivity. Fig. 3.10(b), and (c) show the PDF of signals *Zero* and *One*, and their corresponding BER, for different oversampling rate. It can be

[7]Compared to a coherent receiver, in which the sampling rate and data rate are equal.

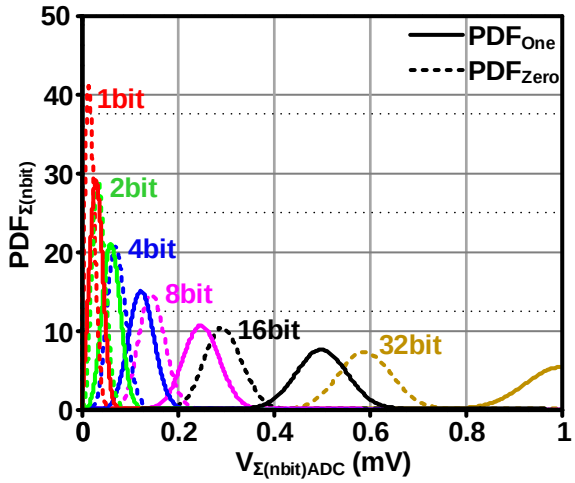
seen that by employing an oversampling rate of 32, the receiver can achieve a sensitivity of -104 dBm[8] at a lower data rate.

This enables the receiver to estimate the power of the incoming signal and if possible adjust and optimize the communication link parameters. For example if the power of the incoming signal drops, the receiver can detect it and ask transmitter to lower the transmitted data rate. Now the receiver can make use of the over-sampled data, accumulate multiple cycles and therefore trade data rate for sensitivity. Having an ADC instead of a comparator also makes it possible to use an adaptive gain control scheme, that improves the dynamic range of the receiver.

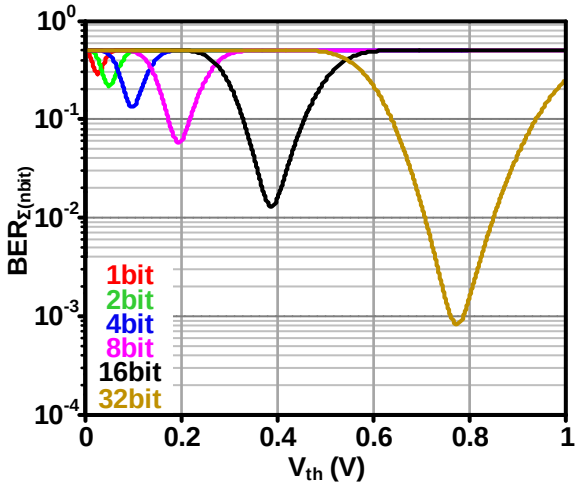
[8]The Quench signal of Fig. 3.18(b) has been used for this simulation, and as will be seen from Fig. 3.22, the oversampling rate of 32 has resulted in $-89-(-104)=15$ dB sensitivity improvement, which is equal to its corresponding theoretical oversampling gain of $10\log 32 = 15$ dB.



(a)



(b)



(c)

Figure 3.10: (a) Baseband data, RF signal and over-sampled data at the receiver, for an 8X over-sampling receiver. (b) The signal Zero and One PDF for accumulation of various number of bits, and (c) the resulting BER for each case. These graph are Matlab simulation results for the actual Quench signal shown in Fig. 3.18(b) and P_{in} = -104 dBm.

3.4 Circuit Implementation

3.4.1 Isolating TransConductance Amplifier (TCA)

The TCA, shown in Fig. 3.11, couples the antenna and SR oscillator. As discussed in Section 3.2, the fundamental functionality of the SR receiver does not hinge on the presence or absence of the input amplifier. Moreover, the noise contribution of the input amplifier, increases the overall NF of the system, degrading the SR sensitivity. It is only the issue of a strong back-radiated signal that mandates employing an input isolating amplifier. A CS-CG architecture provides a single-ended to differential conversion of the input signal without a need for a bulky external (or internal) balun, with an acceptable NF. Assuming $\mathrm{R_p}||\frac{1}{\mathrm{g_{m1}}} \approx \frac{1}{\mathrm{g_{m1}}}$, the thermal noise due to $\mathrm{M_1}$ is canceled at the output. Cascode transistors $\mathrm{M_{3,4}}$, do not contribute to the NF significantly, however they enhance the backward isolation, and increase the output impedance of the TCA, minimizing the loading effect of its output impedance on the SR oscillator tank.

Being part of an ULP system, the input matching cannot be satisfied by means of $\mathrm{M_1}$ transistor, as it would require much more bias current. Therefore inductor $\mathrm{L_1} \approx 14.5\ \mathrm{nH}$ with $\mathrm{Q} \approx 10$ forms the tunable input matching network of the receiver along with the switchable shunt and series capacitor banks $\mathrm{C_{sh}}$ and $\mathrm{C_s}$, and meanwhile provides a path for $\mathrm{M_1}$ bias current.

The transconductance gain of the TCA, $\mathrm{G_{m,TCA}}$, can be found from

$$G_{m,TCA} = 2g_{m1}\frac{V_x}{V_{in}} = 2g_{m1}\underbrace{\sqrt{\frac{R_p||\frac{1}{g_{m1}}}{4R_S}}}_{\approx 1} \approx 2g_{m1} \approx 7\ mmho \tag{3.18}$$

and considering a bias current of $\mathrm{IB_{M_1}}$= $\mathrm{IB_{M_2}}$= 150 μA, $\mathrm{G_{m,TCA}}$ will be about 7 mmho. Assuming a matched input, the total input referred noise power of the TCA is therefore

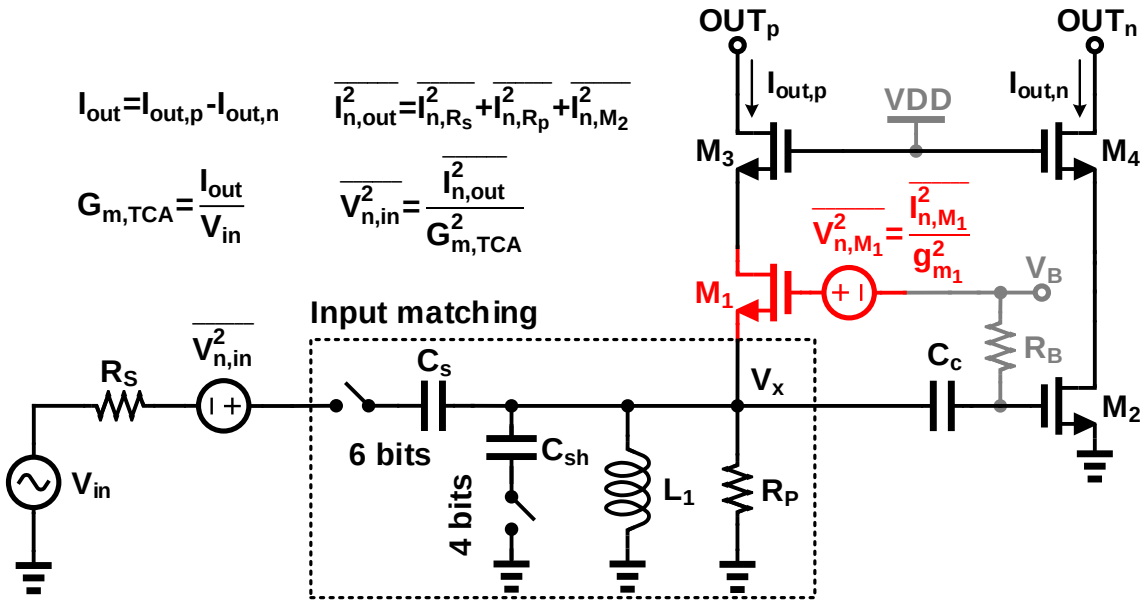


Figure 3.11: Isolation amplifier along with the tunable input matching network. Assuming an acceptable input matching condition, the effect of the M_1 noise, $\overline{V^2_{n,M_1}}$, is canceled at the output.

comprised of the contribution of R_S, R_p, and M_2 as following

$$\overline{V^2_{n,in,TCA}} = 4kT\left(R_S + \frac{R_p}{4\left(1+R_p g_{m1}\right)^2} + \frac{\gamma}{4g_{m1}}\right). \tag{3.19}$$

The simulations also show a backward isolation of better than 70 dB. That is for a stable and continuous 100 mV oscillation at the output of the SRO, the SRR radiates a -80 dBm signal.

3.4.2 Super-Regenerative Oscillator

Being the heart of the SR receiver, it is worth scrutinizing different choices for a SR oscillator. Fig. 3.12 shows three different options for the SRO widely used in SRR design:

1) Differential Colpitts oscillator with bias current switching scheme (Fig. 3.12(a), used in [74])

2) CMOS cross-coupled oscillator (Fig. 3.12(b), employed in [69])

3) NMOS cross-coupled oscillator (Fig. 3.12(c), employed in this design).

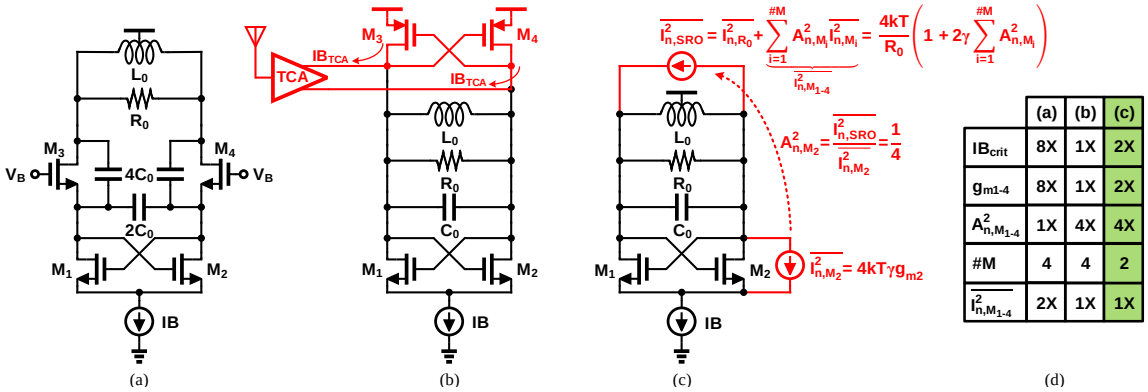


Figure 3.12: Possible choices for the SRO and noise/power comparison. (a) Bias current switching differential Colpitts [74], (b) CMOS cross-coupled [69], and (c) NMOS cross-coupled oscillator. (d) Power consumption and output noise comparison for the presented oscillator choices. The NMOS cross-coupled oscillator is the preferred choice for this design.

Assuming an identical inductor and transistors' aspect ratios in all three cases, the critical current, $\mathrm{IB_{crit}}$, of Colpitts and CMOS cross-coupled oscillators are four times as much and half that of NMOS cross-coupled oscillator, respectively. Therefore, in terms of power consumption, the Colpitts architecture is not an appealing choice for the purpose of an ULP receiver. The total output noise of this stage, $\overline{\mathrm{I}^2_{\mathrm{n,SRO}}}$, is also of importance, and is required to calculate the NF used in (3.6). Considering Fig. 3.12, there are three

types of noise sources contributing to $\overline{\mathrm{I}^2_{\mathrm{n,SRO}}}$; loss of the tank, ie. R_0, thermal noise of transistors M_{1-4}, and the tail bias current IB. Recalling from (3.6) that NF was defined for $\mathrm{IB} \approx \mathrm{IB}_{\mathrm{crit}}$, it can be deduced that the noise associated with the bias current source IB does not contribute to $\overline{\mathrm{I}^2_{\mathrm{n,SRO}}}$, since the SRO is not oscillating and this noise source can be considered a common-mode injection and neglected[9].

We define $\mathrm{A}^2_{\mathrm{n,M_i}}$ as the conversion gain from the thermal noise source of transistor $\mathrm{M_i}$ to the output (as shown in Fig. 3.12(c)), so that $\overline{\mathrm{V}^2_{\mathrm{n,SRO}}} = \sum_{\mathrm{i}=1}^{\#\mathrm{M}} \mathrm{A}^2_{\mathrm{n,M_i}} \overline{\mathrm{I}^2_{\mathrm{n,M_i}}}$, where $\overline{\mathrm{I}^2_{\mathrm{n,M_i}}}$ and $\#\mathrm{M}$ represent the thermal drain noise of transistor $\mathrm{M_i}$[10], and number of transistors in the SRO. Although $\mathrm{A}^2_{\mathrm{n,M_i}}$ for the differential Colpitts is four times smaller than that of cross-coupled counterparts, it has higher $\overline{\mathrm{I}^2_{\mathrm{n,SRO}}}$ due to its higher $\mathrm{IB} \approx \mathrm{IB}_{\mathrm{crit}}$. Fig. 3.12(d) compares the current consumption and output noise of the aforementioned three SRO options. By taking the TCA bias current into account, as shown in Fig. 3.12(b), PMOS transistors $\mathrm{M}_{3,4}$ generate significantly more noise, and consequently the CMOS cross-coupled SRO manifests higher NF. A symmetrical inductor with a differential inductance of $\mathrm{L}_0 \approx 27\ \mathrm{nH}$ and $\mathrm{Q} \approx 13$ is used in the tank, resulting $\mathrm{R}_0 \approx 2\ \mathrm{k\Omega}$, which translates to $\mathrm{IB}_{\mathrm{crit}} \approx 80$, and 40 μA for the NMOS, and CMOS cross-coupled SRO, respectively. Although the NMOS architecture requires slightly more bias current, it can use a lower supply voltage (VDD = 0.65 V in this design) and reduce the overall power consumption, beside manifesting superior NF. The NF of the SR receiver can now be found from

$$NF = \frac{\overline{V^2_{n,in}}}{4kTR_S} = \left(\overline{V^2_{n,in,TCA}} + \frac{\overline{I^2_{n,out,SRO}}}{G^2_{m,TCA}} \right) / 4kTR_S \tag{3.20a}$$

$$= 1 + \frac{R_p/R_S}{4\left(1 + R_p g_{m1}\right)^2} + \frac{\gamma}{4g_{m1}R_S} + \frac{1+2\gamma}{4g^2_{m1}R_0R_S} \tag{3.20b}$$

[9]Due to the inevitable mismatch between the differential transistors of the oscillator, eventually this noise can be translated to differential noise at the output, however with negligible contribution.

[10]Note that since SRO is not oscillating, the flicker noise of transistors does not translate to the higher frequency, and therefore can be neglected at the working frequency or the SRO.

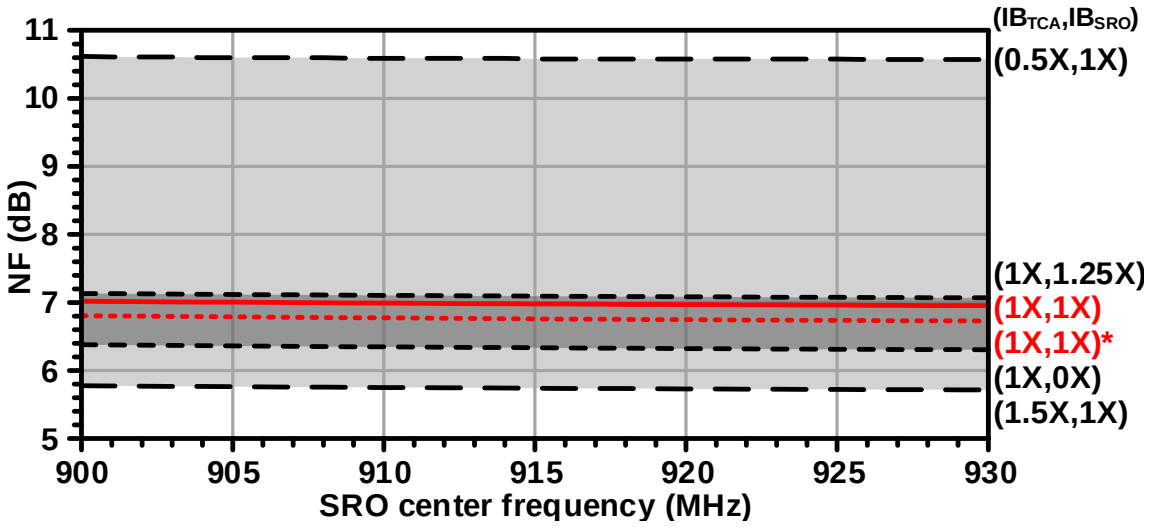


Figure 3.13: Simulated NF of the SRR, measured at the output of the SRO, for different scenarios. The solid red line in the middle shows the NF when TCA is biased at its nominal value $\mathrm{IB_{TCA}} = 150\mu\mathrm{A}$, and the SRO is biased at critical current $\mathrm{IB_{TCA}} = \mathrm{IB_{Crit}}$. The one with asterisk (*), shows the case when tunable input matching network switches are assumed ideal.

to be around 6.2 dB, assuming $\gamma = 1$. Simulated NF of the receiver (at the output of the SRO) is shown in Fig. 3.13, for multiple scenarios of $(\mathrm{IB_{TCA}}, \mathrm{IB_{SRO}})$ pair. When the TCA is biased at nominal bias current $\mathrm{IB_{TCA}} = 150\ \mu\mathrm{A}$, and SRO is biased at its critical current $\mathrm{IB_{SRO}} = \mathrm{IB_{Crit}}$, the NF of the system is about 7 dB. This plot justifies our assumption for (3.6), that NF is weakly dependent of $-\mathrm{G}\,(\mathrm{t})$. As $\mathrm{IB_{SRO}}$ varies from 0 to $\mathrm{IB_{Crit}}$, and finally to $1.25\mathrm{IB_{Crit}}$, and consequently $\mathrm{G}\,(\mathrm{t})$ changes from $\mathrm{G_0}$ to 0, and to $-\frac{\mathrm{G_0}}{4}$, respectively, NF varies for less than 1 dB. This weak relation is expected, since the SRO is the smallest contributing noise source in (3.20a). The tunable matching network introduces about 0.3 dB loss[11], mostly through the on resistance of the series switches.

The final SRO design is shown in Fig. 3.14. The tank consists of a 7-bit capacitor bank, and a varactor, which its control voltage is driven by a 7-bit DAC, for coarse and

[11] That is in TT corner. In worst case scenario of SS corner, the loss increases to around 0.8 dB. Note that to accommodate the low voltage supply, low $\mathrm{V_{th}}$ devices are employed for the switches.

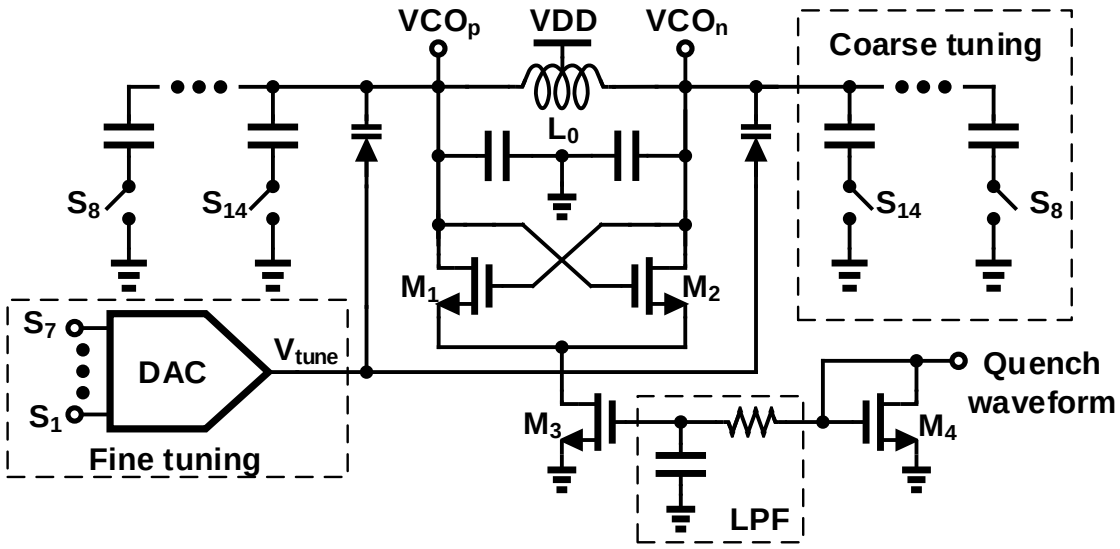


Figure 3.14: Schematic of the designed SRO. Coarse tuning is done through switching a 7-bit binary weighted capacitor bank, while a 7-bit DAC controls two varactor for fine frequency tuning. The fine tuning MSB covers twice the coarse tuning LSB to rid the possibility of frequency gap.

fine frequency tuning, respectively. The MSB step of the fine tuning is designed to cover more than twice as much of the course tuning LSB to ensure there will be no frequency gap, in any various corners, temperatures, and mismatch conditions. The tuning range encompasses $\pm 10\%$ of the center frequency (915 MHz) to ensure that the desired band is completely covered. A fine resolution of around 100 KHz is achieved at the center frequency.

3.4.3 Envelope Detector

A pseudo-differential pair ($\mathrm{M}_{1,2}$) forms a common-mode amplifier with an active load (M_3), as shown in Fig. 3.15. The envelope amplitude of the SRO output signal is amplified through the second-order nonlinearity of $\mathrm{M}_{1,2}$, resulting in a nonlinear gain profile. It is worth noting that due to the exponential growth nature of the SRO output, its envelope has considerably high bandwidth, which should be accounted for in the ED circuitry design. This puts a trade-off on the size of M_{1-3}; smaller transistors expose less parasitics and consequently higher bandwidth and gain, but on the other hand the output voltage suffers from a significant mismatch, and vice versa. A feedback loop along with a replica circuitry is used to set the bias voltage of the ED, as well as to provide a pseudo differential output for the ED. Fig. 3.16 shows the ED input-output characteristics, considering the following stage loading and post-layout parasitics. Monte Carlo simulation for the output bias point shows $3\sigma \approx \pm 50\ \mathrm{mV}$, therefore a 5 bit trimming offset cancellation is added to the output, reducing the offset to around 3 mV.

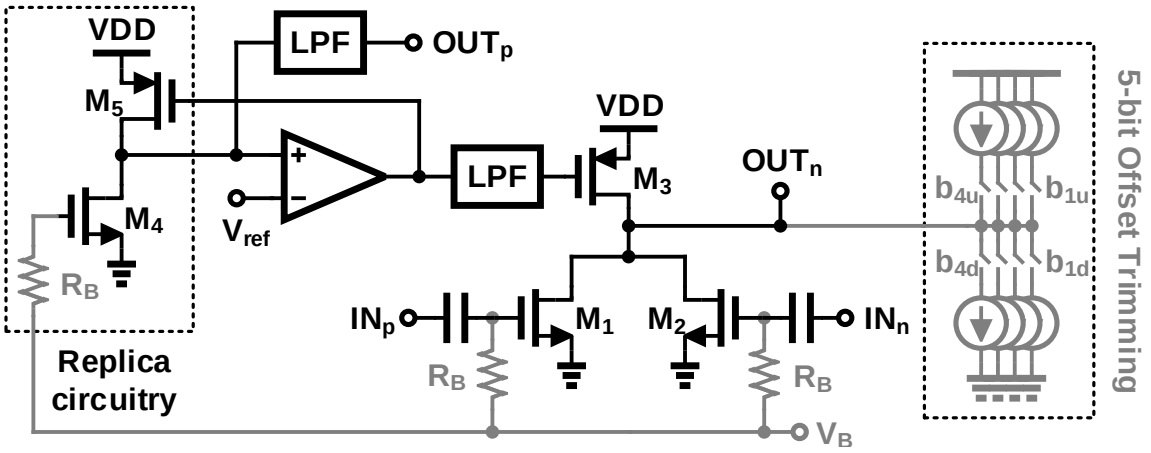


Figure 3.15: Pseudo differential envelope detector circuitry. Two sets of 4-bit source and sink (up and down) switchable current sources form a 5-bit offset trimming scheme.

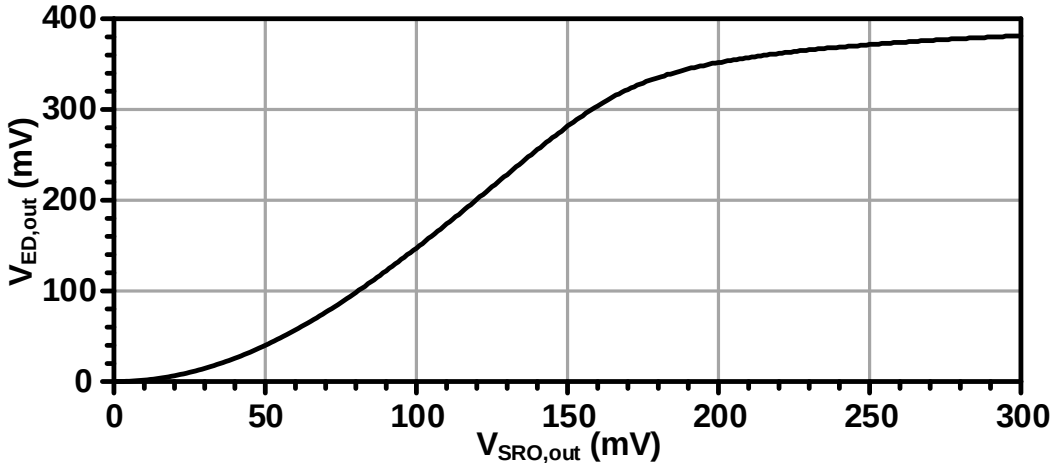


Figure 3.16: The gain profile and input-output characterization of the ED. Dotted lines represent constant envelope, and solid lines show actual SRO envelope as the ED input.

Using the ED input-output characteristics, and knowing its output noise power of $\overline{v_{n,ED}^2} \approx 1.8 \times 10^{-6}\ V^2$, the BER at the output of the ED can be calculated. Fig. 3.17(a), and (b) show Matlab simulation results for the PDF of signals *Zero* and *One*, at the output of the SRO, and ED, respectively, and Fig. 3.17(c), shows their corresponding BER for multiple input signal power level. As it was expected, ED has little to no effect on the BER, since the gain of the preceding stages is considerably high (almost 74 dB). It should also be noted that as long as the ED has a monochromatic gain profile, its nonlinearity does not affect the overall BER.

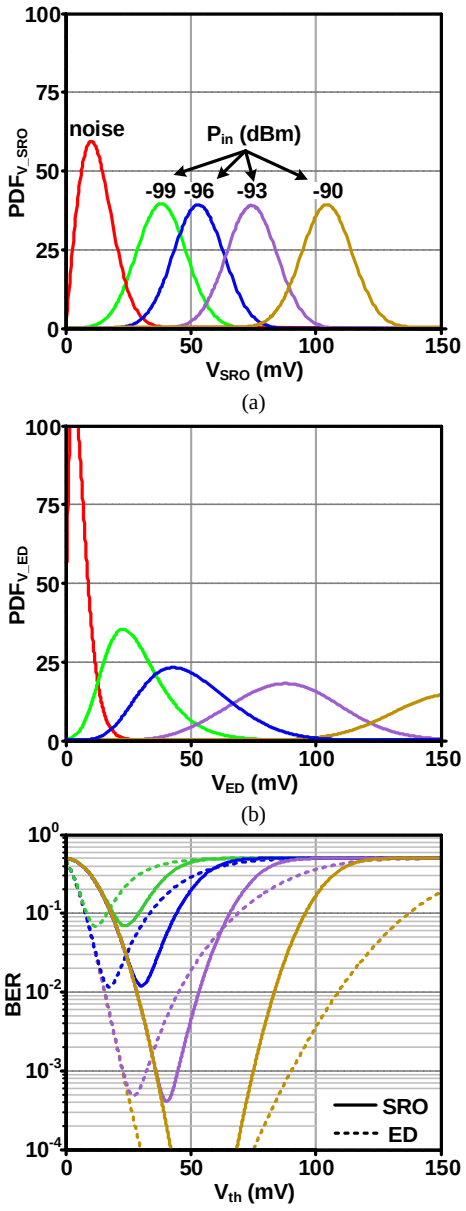


Figure 3.17: (a) the PDF of signals Zero and One, at the output of the SRO for multiple input signal power levels. (b) PDF of the same signals after passing through nonlinear gain profile of the ED and adding the output noise of the ED to them. (c) The BER of the corresponding signals, calculated at the output of the SRO (solid lines), and the output of the ED (dotted lines).

3.4.4 Quench Wave Generator

Fig. 3.5 suggests that the best Quench signal, is the one with zero slope, where $\mathrm{G_i\,(t)}$ is just above zero for most of the cycle, and suddenly jumps to a negative value (Fig. 3.5(a)). However, in reality for an ULP receiver, it is extremely hard to guarantee a stable and precise $\mathrm{G_i\,(t)}$, let alone that the detection of the bias current at which $\mathrm{G_i\,(t) = 0}$ is associated with some intrinsic error. Therefore in this design, performance is compromised in return for robustness. A modified sawtooth waveform is chosen as shown in Fig. 3.18(a), and it is comprised of a pulse and a segmented sawtooth with equal duty cycle, both of which can be tuned with 8 bit accuracy. In this way the performance of the SRR is much less sensitive to the errors in detection of $\mathrm{IB_{Crit}}$, and therefore variations of $\mathrm{G_i\,(t)}$.

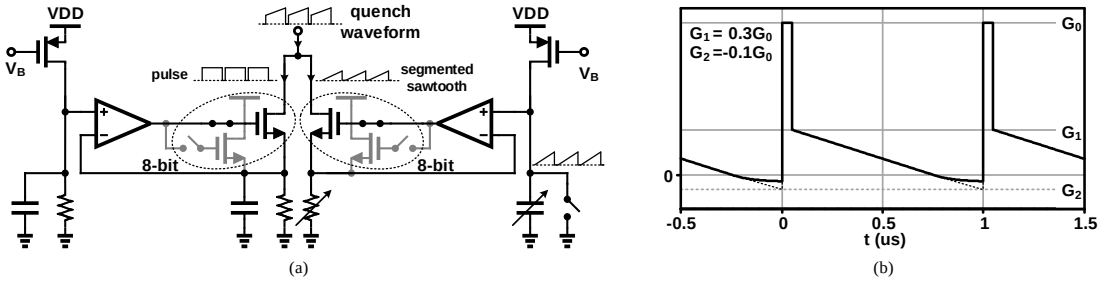


Figure 3.18: (a) QWG schematic; a pulse and a sawtooth generator combined. (b) The actual quench signal used for BER calculation. The linear $\mathrm{G_i\,(t)}$ signal is depicted in dotted line.

So far, it was presumed that $\mathrm{G\,(t)}$ is linearly dependent on $\mathrm{IB_{SRO}}$, however as the oscillation amplitude grows (when $\mathrm{G_i\,(t) < 0}$), the ratio of large signal conductance of the cross-coupled transistors ($\mathrm{G_{LS}}$) to its small-signal one ($\mathrm{G_{SS}}$) starts to drop from initial value of one. Therefore the exact value of $\mathrm{G_i\,(t)}$ not only depends on time but the amplitude of the oscillation. As a result, (3.1) becomes a nonlinear time variant differential equation. Beside the fact that analytical solution for such a system is very complicated

and does not provide intuitive results, $\mathrm{G_i\,(t)}$ and the oscillation amplitude does not have closed form relation and should be estimated from simulations. Therefore an iterative process is taken, to simulate the SRR performance due to nonlinearity of $\mathrm{G\,(t)}$. First a linear $\mathrm{G_i\,(t)}$ model (dotted line in Fig. 3.18(b)) is used to compute (3.13), and its corresponding $\overline{\mathrm{V_{SRO}}}$ is calculated. Provided the value of $\overline{\mathrm{V_{SRO}}}$, an exponentially saturating profile (solid line in Fig. 3.18(b)) for $\mathrm{G_i\,(t)}$ is chosen so that at the end of the quench cycle, $\mathrm{G_i\,(t) = G_0 - G_{LS}}$, where $\mathrm{G_{LS}}$ corresponds to the large signal conductance of the cross-coupled transistors with oscillation amplitude of $\overline{\mathrm{V_{SRO}}}$.

Fig. 3.22 illustrates transient noise simulation results of the designed SRR with $\mathrm{f_q = 1\ MHz}$ and $\mathrm{P_{in} = -87\ dBm}$, along with the analytical prediction of (3.10)-(3.14) with $\mathrm{P_{in} = -89\ dBm}$ using the iterative process explained above, showing an acceptable agreement between the analytical results and transistor level simulations.

3.4.5 ADC

A 5-bit differential SAR-ADC based on [91], as shown in Fig. 3.19, captures the amplitude of the ED output. To accommodate with the low voltage supply of 0.65 V, sampling switches are bootstrapped (Fig. 3.20 [92]), and a double-tail latch-type voltage sense amplifier [93] as shown in Fig. 3.21(a) is also employed as the comparator. Two 4-bit capacitor bank, realized by NMOS transistors, are also added to the pre-charged nodes Di that provide $\pm$15 mV offset cancellation with $\pm$1 mV resolution. A 10 MHz master clock is used to generate all necessary clocks as partly shown in Fig. 3.21(b). The 5-bit output of the ADC is finally registered and stored one cycle to be read.

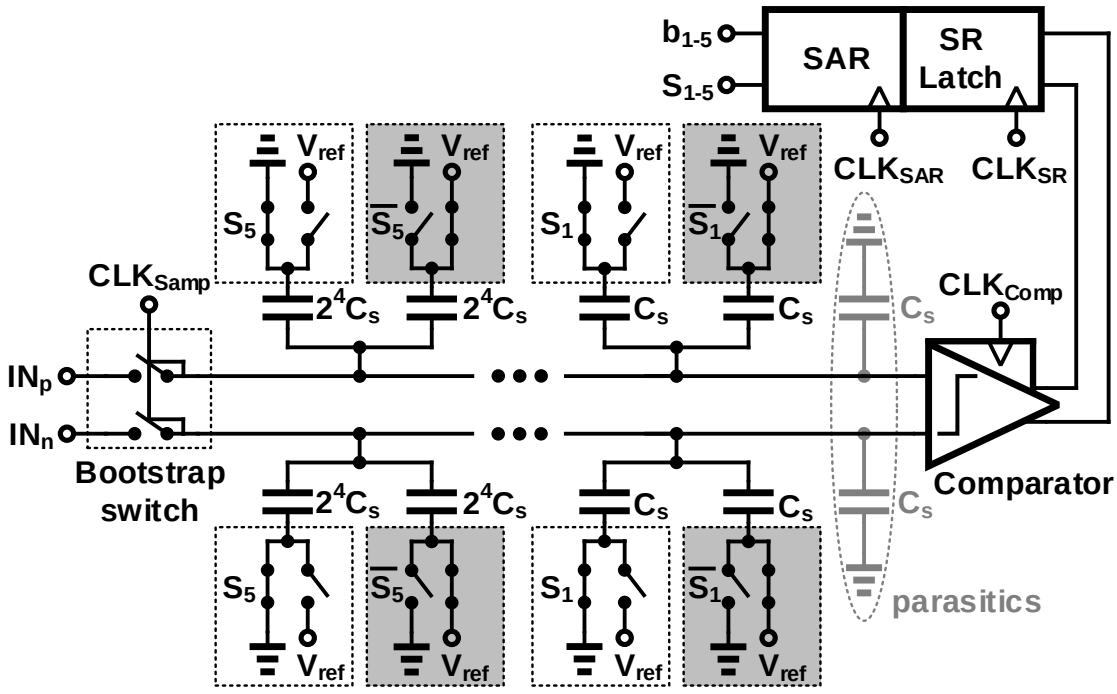


Figure 3.19: 5-bit SAR differential ADC. Parasitics and loading of the comparator input, make up for the non-switchable unit capacitor C_s.

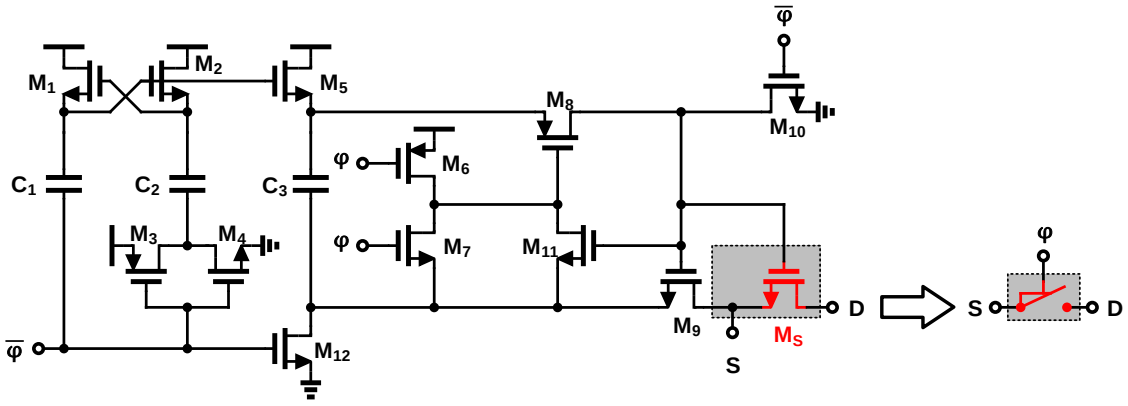
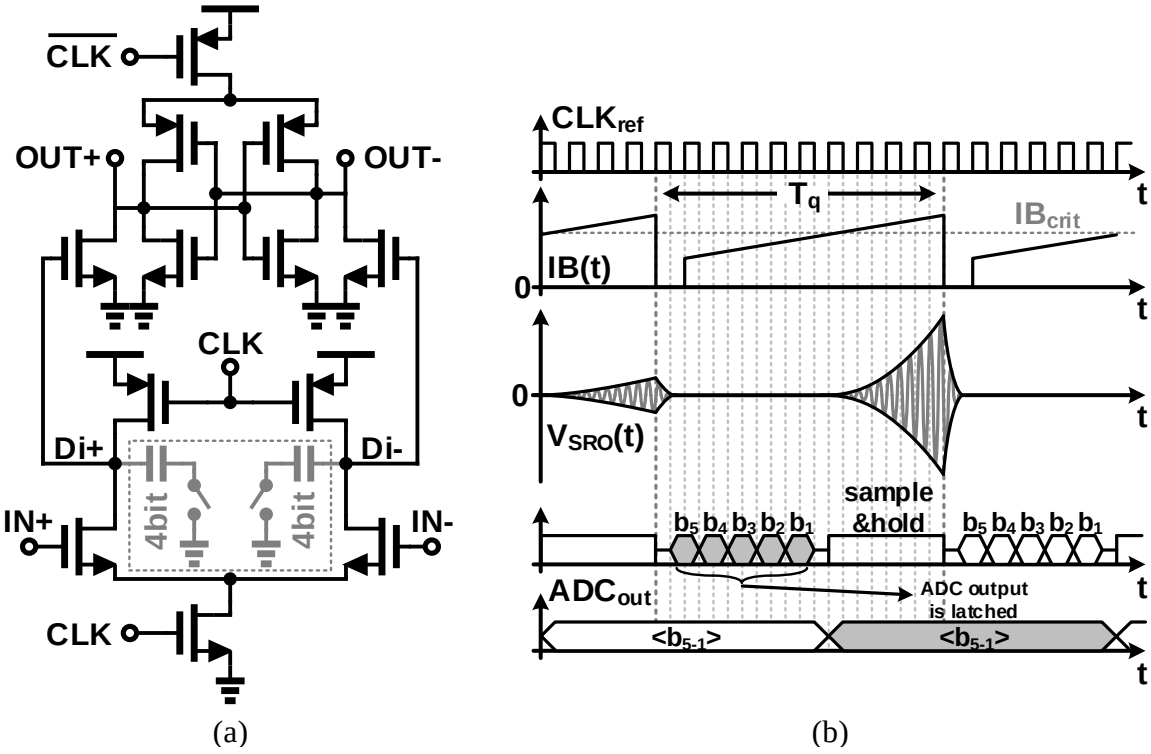


Figure 3.20: Bootstrap circuit and switching device.



(a) (b)

Figure 3.21: (a) Voltage sense amplifier, used as the clocked comparator with 4-bit offset cancellation. (b) Timing of the ADC. After the ED output is sampled at the end of quench cycle, the 5 bits output of the ADC are latched in the next cycle in tandem and latched to be read.

3.4.6 Transient Noise Simulation

Fig. 3.22 illustrates transient noise simulation results of the designed SRR with $f_q = 1$ MHz and $P_{in} = -87$ dBm, along with the analytical prediction of (3.10)-(3.14) with $P_{in} = -89$ dBm, showing an acceptable agreement between the analytical results and transistor level simulations.

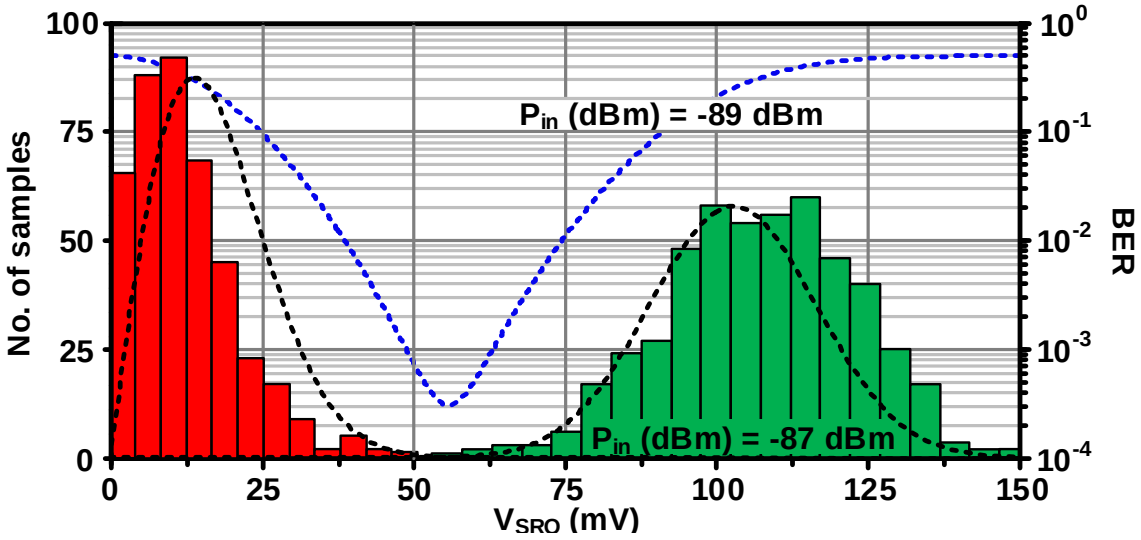


Figure 3.22: The histogram for transient noise simulation of the designed SRR, sampled at the output of the SRO for the input signal $P_{in} = -87$ dBm. The dotted line shows the prediction of the BER for the same system and input signal $P_{in} = -89$ dBm. The mathematical analysis overestimate the sensitivity by about 2 dB.

3.5 Measurement Results

The SR receiver is fabricated in the TSMC 40 nm CMOS technology and occupies an active area of $0.9 \times 0.5\ \mathrm{mm}^2$, as shown in Fig. 3.23, while consuming about 0.5 mA in the RX mode. It also draws less than 1 μA of leakage current when turned off. Table 3.1 summarizes the power breakdown of the SR receiver.

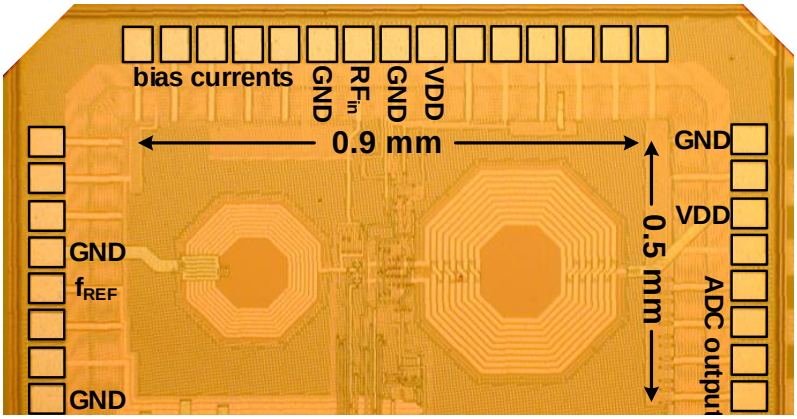


Figure 3.23: Die micro-photograph of the designed SRR.

Table 3.1: Power Breakdown of the Receiver

Individual Block		Operating Mode	
TCA	300 μA	RXM	500 μA
SRO	80 μA	AFC	2.6 mA
QWG	40 μA	CCD	700 μA[1]
ED	50 μA	OFF	< 1 μA
ADC	10 μA		

[1] The exact number varies, depending on the path that binary search takes to complete.

The isolating TCA consumes most of the power, and while it does not play a fundamental role in the performance of the SR receiver (as shown in Section 3.2), it may not be removed. Although [72–74] have removed the isolating amplifier to decrease the power consumption, as explained earlier, this would result in a very strong unwanted back-radiation. It is, however, possible to trade-off sensitivity and power consumption, by decreasing the bias current of the TCA. In this case the NF increases and sensitivity drops. Considering the power breakdown of the receiver in Table 3.1, (3.20a), and Fig. 3.13, and assuming $g_{m1} \propto IB_{TCA}$, it can be inferred that reducing IB_{TCA}, decreases the overall receiver FoM, as defined in (1.1). The back-radiated power of the SR receiver is measured to be around -105, and -90 dBm, in the RX and calibration modes, respectively. The receiver can be tuned from 800 to 980 MHz, fully covering the ISM band of 902-928 MHz. The step size of frequency tuning varies at the high and low end of its range, however at the midband frequency of 915 MHz, it has a resolution of roughly about 35 kHz, achieving 12.5 effective bits of resolution. Fig. 3.24 shows the input return loss of the SR receiver. The back-radiated power of the SR receiver is measured to be less than -105, and -90 dBm, in the RX and calibration modes, respectively.

Fig. 3.25 shows the measured sensitivity of the SR receiver at BER = %0.1, for different data rates. The quench rate is twice the data rate and the quench signal is optimized at each data rate point independently for the best sensitivity, in contrast to [80], in which the optimal quench signal shape at 1 Mb/s was scaled for the rest of data rates, accordingly. As expected, the sensitivity improves at lower data rates. In another approach the sensitivity and data rate, as explained in Section 3.3.2, can be traded off without the need for directly changing the quench rate of the SR receiver. Fig. 3.26 shows the receiver BER versus input signal power, for various oversampling factors, at constant quench rate f_q = 1 MHz. BER improves significantly at higher P_{in} level, and less considerably for very weak input signals, due the exponential relation between BER, and SNR.

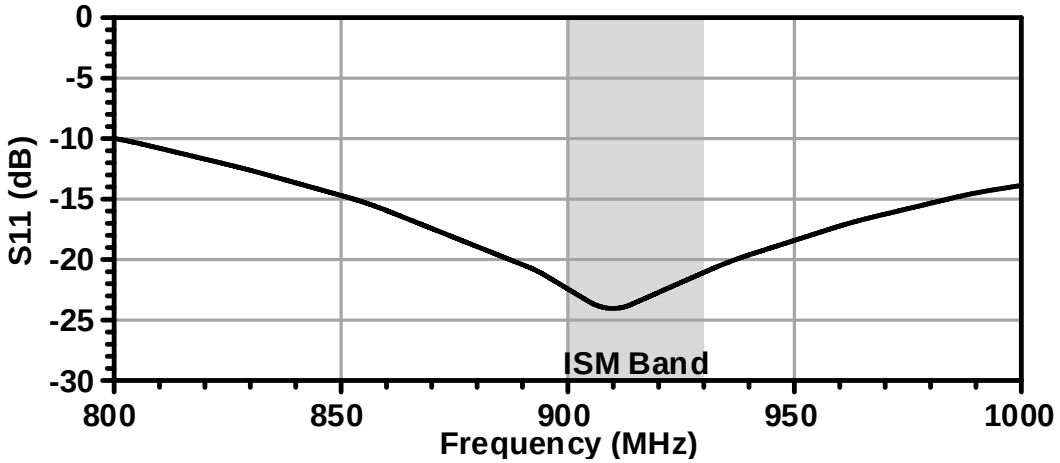


Figure 3.24: Measured SRR input matching after tuning.

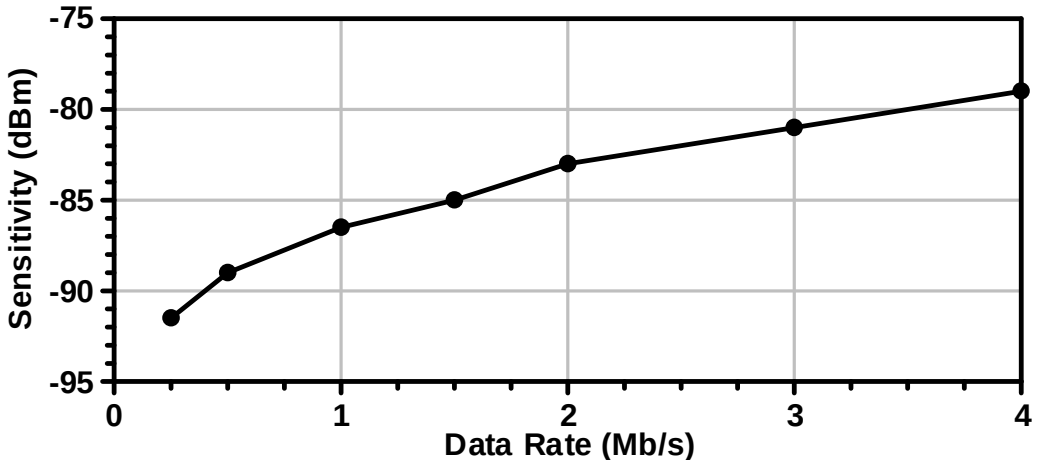


Figure 3.25: Measured Sensitivity versus data rate, while the ADC works as a simple comparator.

Fig. 3.27 illustrates the packet error rate (PER) with a data throughput of 31.25 kb/s, while the receiver quench rate is 1 MHz, versus the signal power. This approach to trade-off data rate for sensitivity is very robust; the quench signal does not need to be optimized for a new data/quench rate. It can be optimized at a single sampling rate, and the ADC data can be used to restore the data at different data rates. Dynamic range of the receiver is

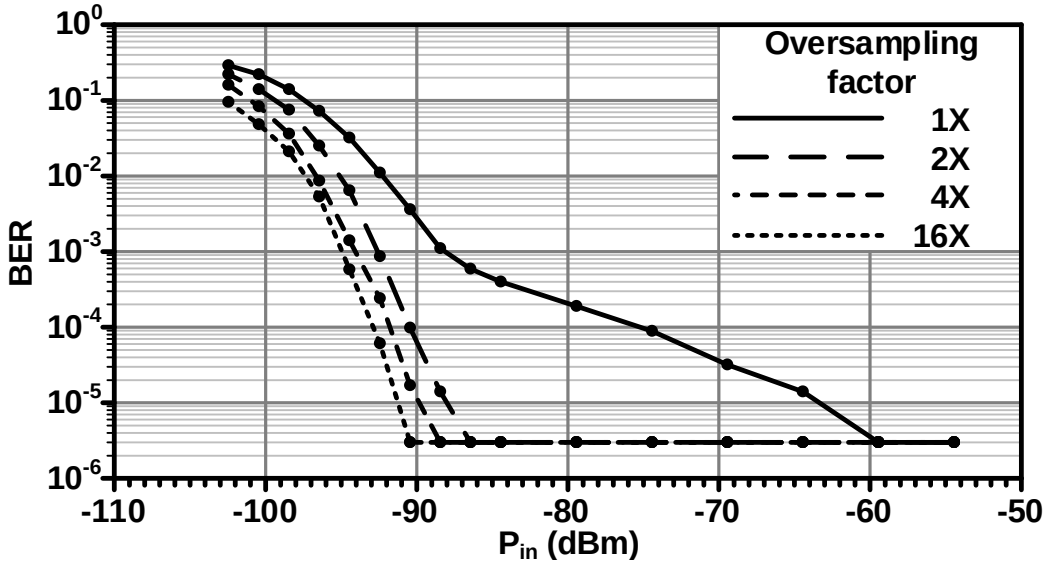


Figure 3.26: Measured BER versus input signal power, for different oversampling factors (f_q = 1 MHz). As expected, oversampling improves the receivers sensitivity, and can be employed to trade-off sensitivity and data rate.

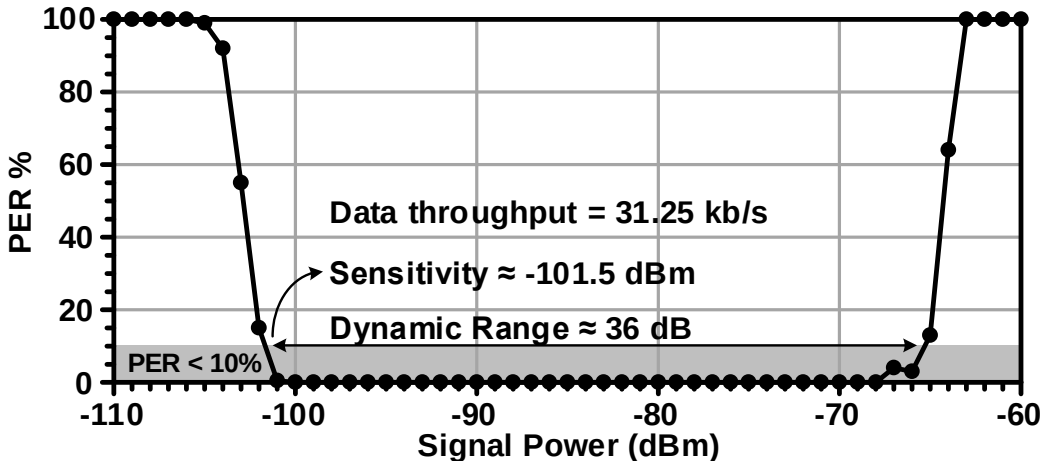


Figure 3.27: Sensitivity-Data rate trade off. The receiver is working with $f_q = 1$ MHz while the data throughput = 31.25 kbps. The output of the ADC is collected and processed to find the PER. The designed SRR maintains a PER below 10% for a dynamic range of about 36 dB, and a minimum signal power $P_{in} = -101.5$ dBm.

limited to 36 dB, and could be improved by incorporating an AGC module within the TCA.

To study the selectivity performance of the designed SRR, a single tone interferer, at different offset frequencies, was applied to the receiver, while the desired signal is at P_{Sens}+3 = -84 dBm with a data rate of 0.5 Mb/s. The receiver is tuned to work at 905 MHz, and the quench rate of 1 MHz. As seen from The Fig. 3.28, the receiver can maintain a BER $\leq 0.1\%$ for an interferer as strong as -50 dBm, when located 10 MHz apart.

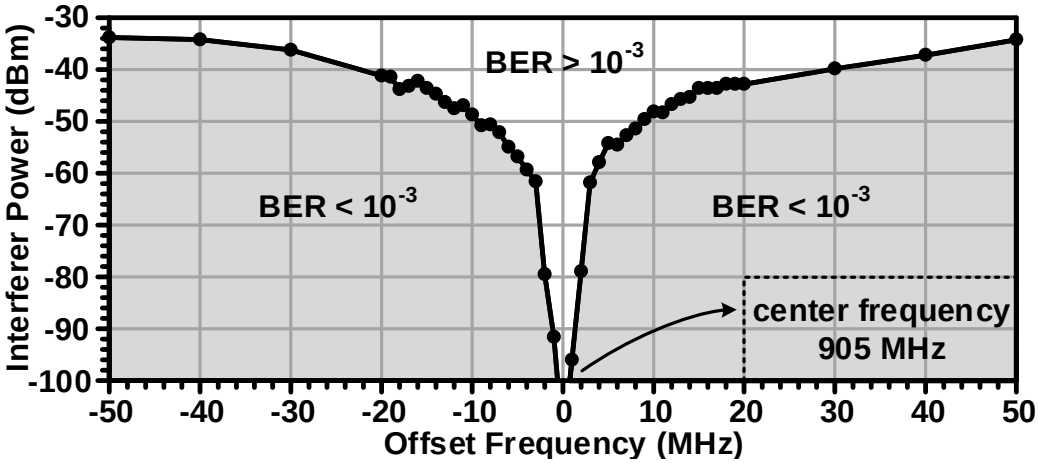


Figure 3.28: Measured interferer rejection versus offset frequency. A single tone interferer was added to the OOK signal at 905 MHz and swept within $\pm$50 MHz, and BER was measured to find the interferer level at which BER falls below 10^{-3}.

It is conceivable that the SRR is incorporated as a Wi-Fi[12] WUR, therefore the wide-band interference behavior of the receiver is of interest. A Wi-Fi signal was generated and placed 20, and 25 MHz apart to emulate a non-overlapping channel interference. The receiver is tuned as described above, and the signal data rate is lowered to 31.25 kb/s. As seen from Fig. 3.29, The receiver can provide up to 43 dB interferer rejection, and tolerate an interferer as strong as -45 dBm.

[12] Although Wi-Fi radio operates mainly in 2.4 GHz ISM band, as seen in Section 3.2, the center frequency of the radio does not play a determining role in the performance of the SRR.

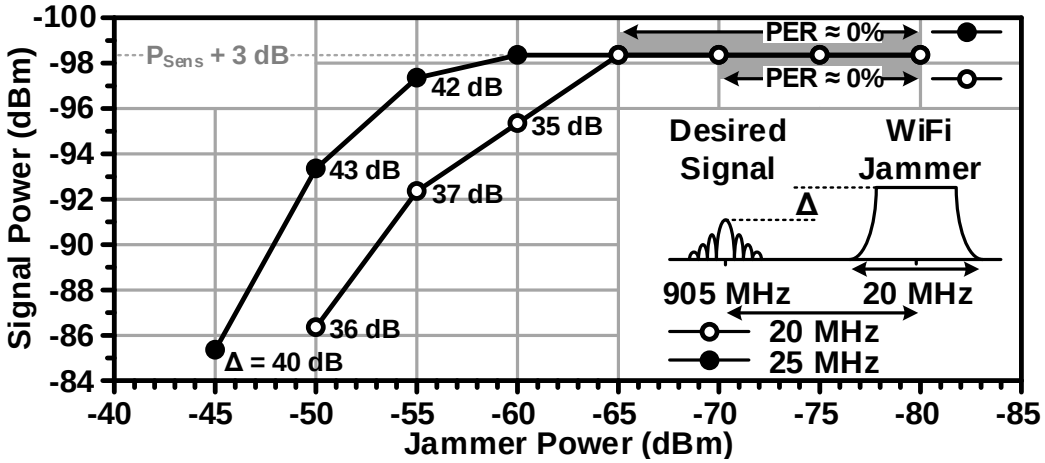


Figure 3.29: Wideband interferer measurement. A wide interferer that emulates a non-overlapping Wi-Fi jammer is added to the desired OOK signal at 905 MHz, and data throughput 31.25 kbps ($\mathrm{f_q} = 1\ \mathrm{MHz}$). The signal and interferer power level is measured for PER $< \%10$, in two cases; 1) the jammer is located 20 MHz apart, in which the Jammer rejection is around 35 to 37 dB, and 2) the jammer is located 25 MHz apart, in which the Jammer rejection is around 40 to 43 dB. For $\mathrm{P_S} = \mathrm{P_{Sens}} + 3 = -98.5$ dBm and jammer power below -70, and -65 dBm the PER ≈ 0, respectively.

Fig. 3.30 shows the offset between the frequency that is set by the calibration scheme, and frequency at which the SR receiver shows its maximum sensitivity. The calibration is being done in two scenarios; 1) the bias current of the SRO is kept constant at $\mathrm{IB_{SRO}} = 1.5$ mA, and 2) The amplitude of the oscillation is kept constant through the ALL at $\mathrm{V_{SRO}} = 50$ mV. In the latter case, since the amplitude of the oscillation is always constant and fairly close to zero, the nonlinear parasitics of the SRO tank circuit do not vary considerably and the offset frequency is comparatively small (below 2 MHz). However in the former case, due to larger oscillation amplitude, the offset is considerably larger. Note that although in the former case the offset is also almost constant, due to PVT variation it might slightly change for different chips or environments, and therefore even a $\%10$ variation can be translated into 2 to 3 MHz of unpredictable offset, degrading the performance of the SR receiver.

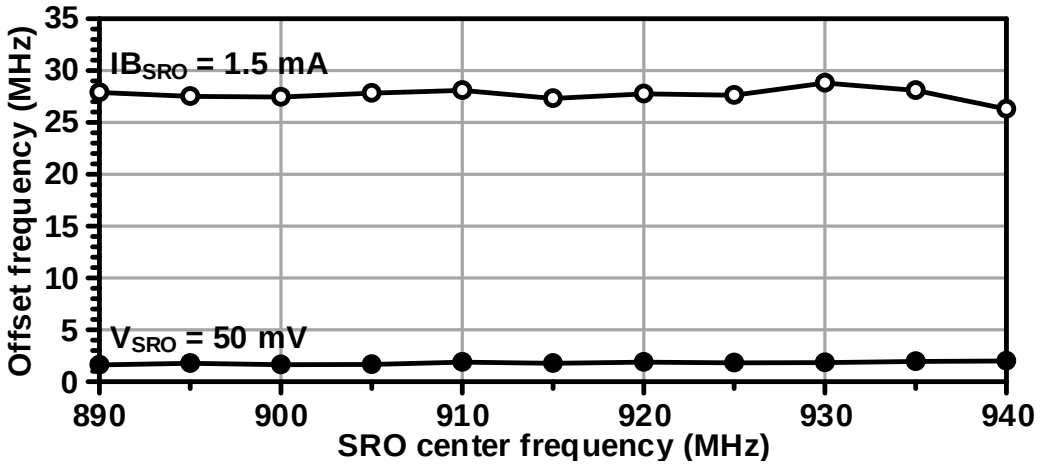


Figure 3.30: The SRO offset frequency, measured in two cases; 1) constant SRO bias current $\mathrm{IB_{SRO}}$ = 1.5 mA, and 2) constant SRO oscillation amplitude $\mathrm{V_{SRO}}$ = 50 mV. The latter case not only results in smaller offset frequency, it has less variation and the calibration phase in this case consumes 10 times less power.

The measurement process was run for about a year and the results and receiver's performance remained consistent over the course of this time. Although the receiver was not measured at extreme thermal conditions, it was mounted on a transceiver board along with a +33 dBm OOK transmitter that increased the ambient temperature considerably. The receiver's performance did not change by turning the transmitter on and off. Table 3.2 compares this work against the state-of-the-art. The Figure-of-Merit (FoM) for this work is calculated for DR = 31.25 kb/s case, and, to the best of the author's knowledge, achieves the highest among reported SR receivers.

Table 3.2: Performance table and comparison to prior works

Publication	[74]	[69]	[73]	[94]	[71]	[78]	[75]	This Work
Year	2009	2011	2010	2015	2013	2011	2007	2016
Frequency (GHz)	0.4	2.4	2.4	2.4	0.4	0.9	2.4	0.9
Architecture	SRO	SRO	SRO	Low-IF	SRO	Inj. Lock	SRO	SRO
SRO resonator	Off-Chip	Bondwire	Bondwire	Off-Chip	Off-Chip	Off-Chip	On-Chip	On-Chip
Intrinsic Q_0	>130	NA	NA	NA[1]	NA[2]	13[3]	10	13
Single-ended RF Input	No	No	No	Yes	No	Yes	No	Yes
Modulation	OOK	OOK	BFSK	OOK	OOK	FSK	OOK	OOK
P_{Sens} (dBm)	-99	-75	-75	-83	-80	-73	-80	-86.5/-101.5
@ DR (kb/s)	40	5000	2000	1000	500	5000	500	1000/31.25
Rejection (dB)	27[4]	NA	20	30	15	12	10	23
@ f_{offset} (MHz)	0.6		15	10	3	5	3	3
@ DR (kb/s)	40		NA	1000	1000	5000	NA	500
Power (μW)	400	534	350	227	123	420	2800	320
Supply (V)	0.8	1.2	0.65	0.6	0.8	0.7	1.2	0.65
Active area (mm^2)	0.5	4.45[5]	0.55	0.8	0.49	1.65[5]	1	0.45
Technology (nm)	90	90	180	65	90	180	130	40
FOM[6]	209	205	207	209	206	204	192	212

[1]Three high-Q inductors.
[2]Two high-Q air coils.
[3]Five low-cost inductors.
[4]$P_{Sig} = P_{Sens} + 6$
[5]Total area including TX.
[6]$FOM = 10 \log (DR/P_{DC}P_{Sens})$.

3.6 Summary

A super-regenerative receiver for ultra-low power applications was presented that in addition to being fully on-chip, to the best of the authors knowledge, achieves the highest FoM, among ULP receivers. Mathematical modeling and in-depth analysis of an SR oscillator behavior and, from that, an SR receiver was presented. This analysis enables one to estimate the receiver's BER at a given signal power, or sensitivity at a given BER. The receiver is designed to work with On-Off Keying (OOK) modulation at variable data rates from 0.5 up to 4 Mb/s, and exploits low-voltage techniques to work with a 0.65 V supply, resulting an excellent energy efficiency of 80 pJ/b at the 4 Mb/s data rate with a sensitivity of -76 dBm. An integration-oriented design has resulted in a receiver without either external inductor or balun. Furthermore, different calibration schemes improve the robustness of the SRR performance, and by precise controlling a modified saw-tooth feedback signal, an enhanced Q of 1500 is achieved. The receiver is using a 5-bit ADC to determine the amplitude of the incoming signal instead of a simple comparator, and this has enabled the receiver to trade-off data rate for sensitivity in the baseband post-processing stage, achieving an excellent sensitivity of -102 dBm at 31.25 kb/s data rate and 43 dB wideband interferer rejection.

4. CONCLUSIONS

In previous chapters we described two different area of interest in RF receiver design area; cognitive radio that exploits vacated TV bands to establish long-distance high-speed data links, and ULP receiver that can be employed for WSN, WUR, MICS, or IoT applications. As discussed in Chapter 2, the main purpose of this design is to come up with a receiver that is suitable to be used for the low end of the CR band. This particular standard (i.e. IEEE 802.22) is developed mainly to provide high speed Internet access to rural areas that lack modern infrastructure (such as optical fiber), using already existing video broadcasting base stations. As mentioned in section 2.1, the lower end of the spectrum is more appealing due to its higher propagation properties, meaning a given base station can cover wider range of area (as it is expected to cover up to 100 km), or provide higher quality signals for closer customers.

Therefore the targeted design should cope with the harmonic mixing problem as it can potentially be the most destructive issue for this particular standard, for the reasons explained in details in section 2.2. our approach was to deal with this issue as the top-most priority, all the same, maintain an acceptable and comparable to the state-of-the-art performance in terms of linearity and NF. The first goal was achieved by employing an up-down heterodyne conversion scheme. As explained in section 2.3, this architecture pushes the harmonics and potential image signal to frequencies well beyond the receiving band, making it possible to attenuate them considerably, regardless of their harmonic number. Using this up-down heterodyne scheme, to cope with harmonic mixing issue, is not a new technique. However, what other published works lack is providing measures to improve linearity of this system. As discussed in section 2.2, out of band interference due to non-linearity of the receiver can also play a considerably destructive role. Therefore an active

feedback is also employed within the receiver chain to enhance the linearity. The linearity enhancement is also studied in great details, and through rigorous modeling, simulations and measurements, its efficacy has been shown. It is worth noting that active feedback, and heterodyne conversion are well-known architectures, but to the best of my knowledge, they had not been combined in a single receiver, and their combined performance had not been studied. Moreover, among the recent works that have employed heterodyne architecture to address the harmonic mixing issue, they either did not put emphasis on linearity improvement [41, 42] or if they did, they did not achieve their goal [40].

The presented design, in its current form, suffers from a poor NF performance. There are however simple solutions (in terms of cost, power and complexity overhead) that can potentially improve the NF, at least to some marginal extent:

1. For instance, using a higher technology node, as explained in section 2.7, makes it feasible to increase the LNA gain, without worrying about its bandwidth and therefore stability of the feedback loop. Please note that compared to most of the cited references, this work uses a much longer feature size technology, while most of the state-of-the-art designs are benefiting from better technology.

2. In addition to moving to a higher technology node to improve the performance, the receiver's NF performance can be improved by breaking its operating frequency into two bands. The higher end of the band can exploit direct conversion scheme, similar to those cited in Table 2.4. As explained in section 2.7, a direct conversion architecture that employs a 3^{rd}, and 5^{th} harmonics rejection scheme can work pretty well for frequencies above roughly 400 or 500 MHz. The lower end can employ the presented up-down heterodyne conversion. In this case even without migrating to a higher technology, a higher gain LNA is feasible, since the bandwidth is less, and therefore the NF can be improved.

It should also be noted that the presented work, although is comprised of various well-known architecture, is tailored together in a new fashion that provides almost a unique performance. It provides high linearity and high harmonic rejection for all the harmonics simultaneously. This design lacks good NF, and it was the price to achieve the targeted performance (i.e. simultaneous linearity and harmonic rejection). However, it is worth emphasizing that for this particular standard and application, harmonic rejection should be recognized as a merit of a receiver performance, when it comes to the state-of-the-art comparison.

In Chapter 3 also, we discussed the need for ULP receivers and reviewed the state-of-the-art. There are four architectures that are mainly adopted to realize an ULP receiver, although for sub-mW applications, super-regenerative, and uncertain IF based receivers dominate the field. Since an UIF receiver lacks a modest interference resilience and as shown if Fig. 3.2 does not offer a better FoM (as described in (1.1)), super-regenerative technique was chosen to realize the targeted ULP receiver.

Section 3.2 presents a comprehensive mathematical analysis of super-regenerative behavior, and showed how shape of the Quench signal affects the performance of a SR system. In this section we established a method to relate the circuit-level characteristics of the receiver, such as gain, NF, and shape of the Quench signal, to the receiver's overall performance, in terms of sensitivity and BER.

It was stated that ULP receivers, generally, lack selectivity and robustness. In contrast to linear receivers where a PLL is continuously working and generating a precise LO signal which down-converts the desired frequency, an ULP receiver, mostly, relies on calibration schemes that are working periodically. Section 3.3 introduced two calibration loops that are employed in this design to guarantee the proper performance of the receiver. Firstly, an AFC loop sets the operating frequency, taking into account the inevitable offset frequency, between the measured and desired frequency. Secondly, a CCD loop searches for and

detects the critical current of the SRO, so that the QWG module can be programmed accordingly. It was shown by measurements that using an amplitude lock loop while running AFC minimizes the calibration power consumption and the incurred offset.

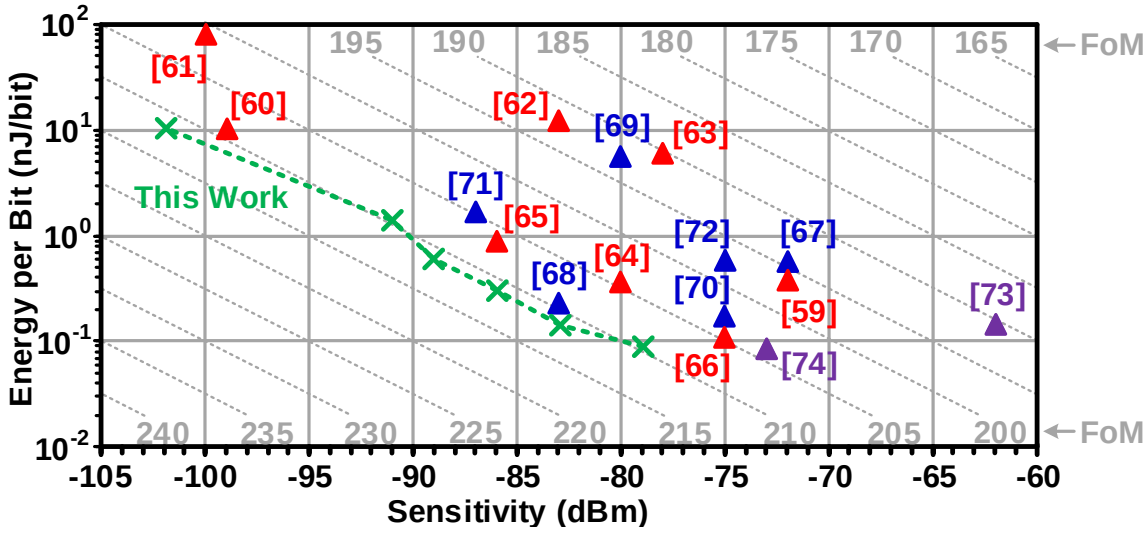


Figure 4.1: Performance of this work (green line) against the state-of-the-art; SRR (red data points), UIF (blue data points), and ILO (violet data points) family.

Also, the receiver is designed to be integration-oriented, meaning it does not use or need any external component. As seen in section 3.2, quality factor of the SRO tank circuit plays a major role in the performance of the receiver. For instance, [71, 74, 78, 94], have used high quality off-chip resonators to achieve quality performance. Fig. 4.1 compares the performance of the proposed receiver, against the state-of-the-art. Despite the fact that this design does not benefit from high-quality off-chip component, it excelled at the FoM. Moreover, This receiver can offer its high FoM over a wide range of sensitivity-data rate trade-off. The latter was accomplished by employing an ADC as a mean to interpret the incoming signals strength instead of a simple comparator. This enables the receiver to compromise data rate for sensitivity (and vice versa). For instance, the receiver can extend

its sensitivity level beyond -100 dBm, by lowering the throughput data rate; a lower rate data can be spread over a much higher baud rate stream. This has enabled the receiver to detect a -102 dBm signal with throughput 31.25 kbps.

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APPENDIX A

ACTIVE FEEDBACK LOOP NONLINEARITY MODEL

In Section 2.4.1 we established a simple model to calculate the interferer rejection of the active feedback loop shown in Fig. 2.5. Here we scrutinize in more depth the effect of nonlinearities of the active feedback loop and the limited filtering power of the LPF in the feedback path.

As mentioned earlier, the fundamental tones in the loop are not affected by the nonlinearity of the blocks, except for the compression effect that is negligible. Therefore to find the level of fundamental tones, recalling from the linear control system, we can use the following equation for the block diagram shown in Fig. A.1

$$A_{node\ n} = \frac{Forward\ Path\ Gain\,(\omega)}{1 + Loop\ Gain\,(\omega)} A_{in} \tag{A.1}$$

in which loop gain is

$$T(\omega) = \frac{\alpha_1 \beta_1 \delta_1}{\sqrt{1 + \left(\frac{\omega - \omega_{I1}}{\omega_c}\right)^2}} = \frac{T_0}{\sqrt{1 + \left(\frac{\Delta\omega}{\omega_c}\right)^2}} \tag{A.2}$$

where ω_c is the cut-off frequency of LPF, and $\Delta\omega = |\omega - \omega_{I1}|$ is the offset frequency between the signal and interferers. Assuming that the amplitude of the two interferer tones at the input (node x) are both equal to A_I, we can find the amplitude of the fundamental

tones at node e, y, and b as following

$$A_{I1,e} = \frac{1}{1+T_0} A_I \tag{A.3a}$$

$$A_{I2,e} = \frac{1}{1+T(\omega)} A_I \tag{A.3b}$$

$$A_{I1,y} = \frac{\alpha_1}{1+T_0} A_I \tag{A.3c}$$

$$A_{I2,y} = \frac{\alpha_1}{1+T(\omega)} A_I \tag{A.3d}$$

$$A_{I1,b} = \frac{\alpha_1\beta_1}{1+T_0} A_I \tag{A.3e}$$

$$A_{I2,b} = \frac{\alpha_1\beta_1 T(\omega)}{(1+T(\omega))\, T_0} A_I. \tag{A.3f}$$

with the same token, the amplitude of the signal at the output (node y) can be calculated from

$$A_{S,y} = \frac{\alpha_1}{1+T(\omega)} A_S = \frac{\alpha_1}{1+\frac{T_0}{\sqrt{1+\left(\frac{\Delta\omega}{\omega_c}\right)^2}}} A_S. \tag{A.4}$$

The IM3 terms component on the other hand are only produced when the fundamental tones pass through a nonlinear block. Therefore we can introduce the IM3 terms that each block generates by adding them at the output of that block as shown in Fig. A.1. We can again use (A.1) to find the final IM3 term at the output

$$A_{IM3,y} = \frac{A_{IM3,LNA} - \alpha_1 A_{IM3,UM2} - \frac{T(\omega)\delta_1\alpha_1 A_{IM3,DM2}}{T_0}}{1+T(\omega)}. \tag{A.5}$$

Knowing the fundamental tones at each node from (A.3), the IM3 term that each block

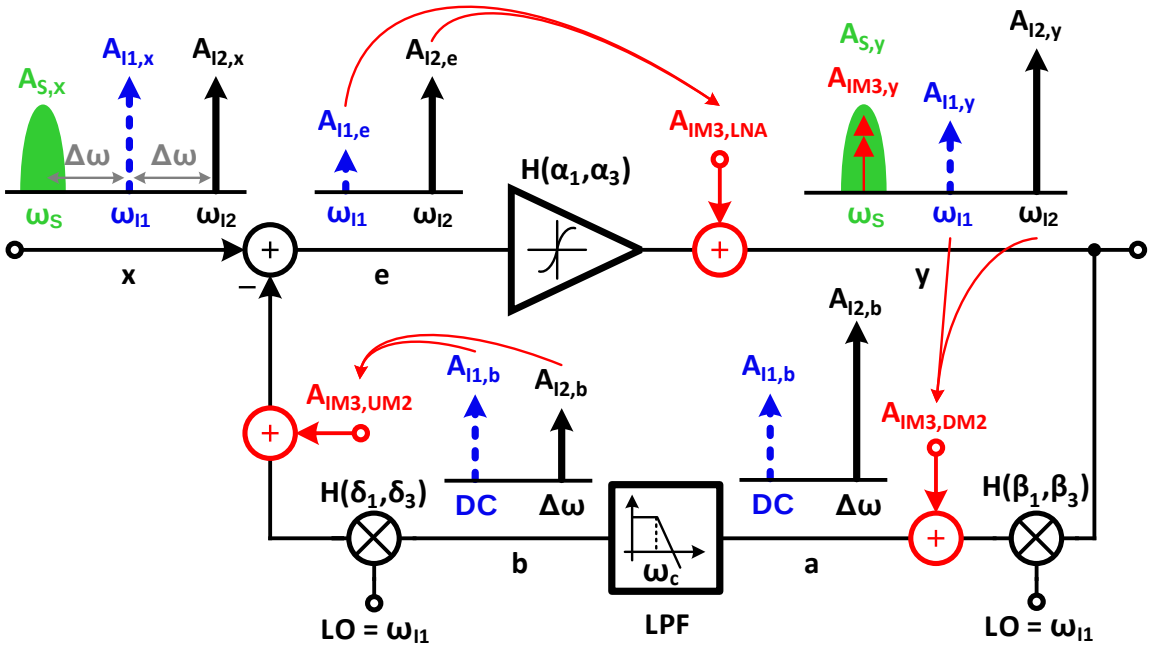

Figure A.1: The active feedback loop considering the nonlinearity and non-idealities of different blocks in the loop.

generates can be calculated

$$A_{IM3,LNA} = \frac{3}{4}\alpha_3 A_{I1,e}^2 A_{I2,e} \tag{A.6a}$$

$$A_{IM3,UM2} = \frac{3}{4}\delta_3 A_{I1,b}^2 A_{I2,b} \tag{A.6b}$$

$$A_{IM3,DM2} = \frac{3}{4}\beta_3 A_{I1,y}^2 A_{I2,y}. \tag{A.6c}$$

Substituting (A.6) and (A.3) into (A.5), the final IM3 term at the output of the loop in

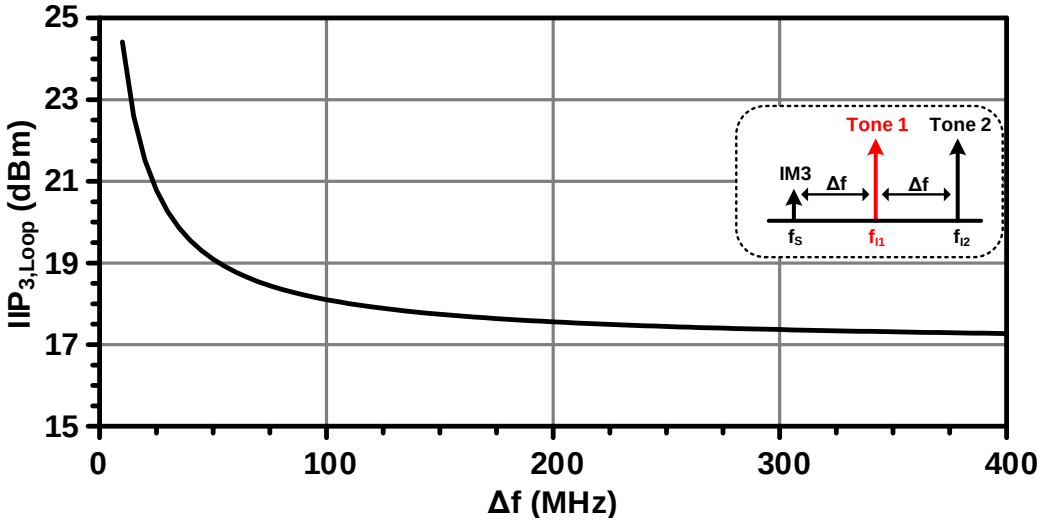

Figure A.2: The simulated IIP3 of the active feedback loop, based on the model presented in the Appendix and design parameters in Section 2.5.2. Note that since the output of the feedback system is considered at the output of the LNA, $\mathrm{IIP}_{3,\mathrm{LOOP}} = \mathrm{IIP}_{3,\mathrm{LNA}}$ when the LNA is inside the active feedback loop.

terms of the interferers amplitude and system parameters can be found as

$$A_{IM3,y} = \frac{3}{4}\left(\frac{1}{1+T(\omega)}\frac{1}{1+T_0}\right)^2 \times \left(\alpha_3 - \frac{\alpha_1\beta_1}{\sqrt{1+\left(\frac{\Delta\omega}{\omega_c}\right)^2}}\delta_3 - \alpha_1^3\beta_3\right) A_I^3 \tag{A.7a}$$

$$\approx \frac{3}{4}\left(\frac{1}{1+T(\omega)}\frac{1}{1+T_0}\right)^2 \left(-\alpha_1^3\beta_3\right) A_I^3. \tag{A.7b}$$

As was shown in Fig. 2.6, gain of the LNA from single-ended input to the output is 3 dB more than that of seen through differential feedback loop, ie. α_1, therefore the input referred amplitude of the final IM3 term can simply be found from

$$A_{IM3,in} = \frac{A_{IM3,y}}{\sqrt{2}\alpha_1}. \tag{A.8}$$

Now assume two interferers with amplitude A, passing through a nonlinear system, where the input referred amplitude of the resulting IM3 term is $\mathrm{A_{IM3_{in}}}$, in this case we can use the following equations to find the $\mathrm{IIP_3}$ of that system

$$A_{IM3_{in}} = \kappa A^3 \tag{A.9a}$$

$$A_{IIP_3} = \frac{1}{\sqrt{|\kappa|}} \tag{A.9b}$$

$$IIP_3 = 10 - 10\log|\kappa|\,. \tag{A.9c}$$

Using (A.7) to (A.9), we can compute the overall IIP3 of the feedback loop as illustrated in Fig. A.2. Note that in other words Fig. A.2 shows the linearity of the LNA when embedded inside the active feedback loop which was referred to in (2.10). As can be seen in this figure at very low offset frequencies, the IIP3 increases sharply. The reason for that is, at very low offset frequency, the second interferer also gets attenuated in the loop, and consequently the overall IIP3 increases. That is in contrast with very large offset, where the second interferer does not experience the excursion around the loop as LPF filters it out. It is also important to note that at low offset frequencies, the desired signal also gets attenuated more, resulting in excessive NF degradation, as can be seen in Fig. 2.20.